

A study on performances of carrier-based pulse-width modulation techniques for three-phase three-level t-type neutral-point-clamped inverter under switch-open-circuit fault on two neutral-point-connected legs

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ABSTRACT

Multilevel voltage source inverters (VSIs) have been used for several decades thanks to their advantages compared with traditional two level VSI. Among various types of multilevel configuration, the T-type neutral-point-clamped VSI (3L TNPC VSI or 333-type VSI) has gained the attention in recent years. Due to the unique structure, the 333-type VSI has critical issues in reliability in operation such as switch-open-circuit (SOC) and switch-short-circuit (SSC), which lead to several unrequired issues, for instance, reduction of system performance, distorted and unbalanced output voltages and currents, or triggering the protection circuits. In some applications, the amplitude reduction and harmonics distortion of output voltages in SOC faults are not acceptable. Therefore, it is necessary to develop a pulse-width modulation (PWM) algorithm for 333-type VSI working under SOC fault which guarantees the desired output fundamental component voltage. The simultaneous SOC fault on two neutral-point-connected legs in the 333-type VSI may cause a large reduction in the output voltage. Under this circumstance, the 333-type VSI becomes an asymmetrical one called 322-type VSI. Certain studies regarding to the operation of 333-type VSI under SOC faults have been carried out. However, these studies require more semiconductor devices in order to create a redundant switching circuit. This leads to higher system cost with reduced inverter efficiency due to the additional loss. In this study, two carrier-based pulse-width modulation (CBPWM) techniques, i.e. 322-sinusoidal PWM (322-SPWM) and 322-medium offset CBPWM (322-MOCBPWM) are proposed for 322-type VSI. The proposed techniques are firstly simulated in MATLAB/Simulink and then implemented on a hardware setup. Performances of the proposed techniques are evaluated in terms of total harmonic distortion (THD) and weighted-THD (WTHD) of output voltages. Simulation results show that considering the worst output voltage under SOC fault, vBC, the proposed 322-SPWM technique could improve the THD by 40% and the WTHD by 94% compared with the uncompensated case with $m=0.8$. The corresponding results of 322-MOCBPWM technique are 42% and 96%, respectively. Characteristics of THD and WTHD values are also presented for demonstration the effectiveness of the proposed algorithm.

Key words: Carrier-based pulse-width modulation, t-type neutral-point-clamped inverter, switch-open-circuit fault, voltage source inverter, weighted-total harmonic distortion

INTRODUCTION

Multilevel inverters (MLIs) have been being researched for nearly forty years since the first introduction of three-level neutral-point-clamped (3L NPC) voltage source inverter (VSI) in 1981^{1,2}. Compared with traditional two-level VSI (2L VSI), 3L NPC VSI offers a larger number of benefits. For instance, 3L NPC VSI has lower distortion of output voltage and dv/dt, lower distortion of input current, smaller magnitude of common-mode voltage (CMV) or even elimination of CMV by using some sophisticated modulation methods, and ability in operation with a lower switching frequency¹⁻⁷. Among with many

types of 3L NPC topology, 3L T-type NPC (3L TNPC) topology has an advantage in terms of efficiency compared to 3L NPC⁵. For example, 3L TNPC VSI possesses higher efficiency in low-voltage applications for the switching frequency between 4-25 kHz such as photovoltaic (PV) system, uninterruptible power supplies (UPSs), and automotive converter system^{5,8,9}. 3L TNPC VSI combines the benefits of both 2L VSI and 3L NPC VSI, such as lower conduction losses, lower switching losses and higher output power quality⁸. The TNPC topology also allows the usage of lower voltage rating power switches and offers considerably power losses compared with that of NPC topology^{5,8}.

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However, due to the use of total 12 power switches topology, the reliability of 3L TNPC VSI inverter is an important issue which is related to the cost and efficiency of the overall system⁸. It is summarized that there are two typical types of failure that may occur in semiconductor switches in a power inverter, which are switch-short-circuit (SSC) fault and switch-open-circuit (SOC) fault, respectively⁸⁻¹⁰. SSC faults often come from the over-voltage, over-current, avalanched stress or over-thermal issues, which could result in serious damage to the switching devices due to the abnormal overcurrent^{8,9}. Typically, the inverters stop operation after the detection of SSC fault for safety reason¹⁰. In contrast, SOC faults occur due to malfunction of gate driver circuits or the lifting of bonding wire caused by thermal cycling⁸⁻¹⁰. Although SOC faults do not lead to serious damage to the inverter compared with SSC faults, the system performance will deteriorate in SOC fault. In addition, SOC fault leads to current distortion of output, secondary issues in other components in the topology such as gate drivers and other IGBTs by means of noise and vibration⁸. The asymmetrical and distorted current caused by SOC fault may saturate transformer, trigger circuit protection¹⁰. Moreover, SOC faults could reduce the fundamental component of output voltage which is not allowed in certain voltage-sensitive applications, for example, UPS of PV systems¹¹. Therefore, a modulation algorithm for 333-type VSI working under SOC faults should be developed to guarantee the desired fundamental component of output voltages as well as the balanced output currents.

Figure 1(a) shows the topology of 3L TNPC VSI under normal operation while Figure 1(b) and Figure 1(c) show that under SOC fault on one neutral-point-connected leg and two neutral-point-connected legs, respectively. The topology in Figure 1(b) is called 332-type VSI while that in Figure 1(c) is 322-type VSI.

Certain studies on pulse-width modulation (PWM) techniques implemented on 333-type VSI under SOC fault conditions on neutral-point-connected legs were carried out at⁸⁻¹¹. Study conducted by U. Choi *et al.*⁸ proposed a diagnosis and tolerant algorithm for SOC fault considering two types of SOC fault which occurring in neutral-point-connected bridge and in the main bridge. In case of SOC fault on neutral-point-connected leg, the proposed technique in this study was based on SVPWM algorithm and had the capability in elimination of harmonic distortion in output current⁸ resulting more reliability in 333-type VSI which could be implemented in servo and PV systems. Besides, this solution did not require any additional switches. S. Xu *et al.* investigated a fault-tolerant topology and control strategy of 333-type

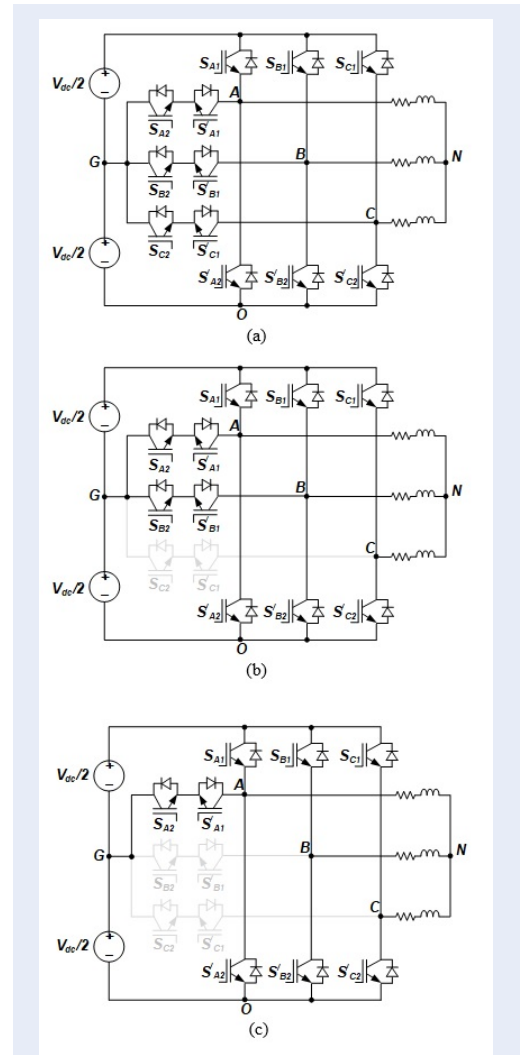


Figure 1: Topologies of 3L TNPC VSI: (a) In normal condition (333-type VSI); (b) In SOC fault on one neutral-point-connected leg (332-type VSI); (c) In simultaneous SOC faults on two neutral-point-connected legs (322-type VSI).

VSI under different fault conditions including SOC faults on neutral-point-connected switch with ride-through capability as well as maintained high-quality output⁹. However, this solution required a fourth redundant leg which could increase the system cost and power losses. Similarly, the solution proposed by J. He *et al.*¹⁰ also used a redundant phase-leg yet utilized advanced switching techniques such as zero-voltage switching (ZVS) and zero-current switching (ZCS), thus relieved the thermal stress on switches and improved system efficiency while maintain the desired output voltage and output power. On the other hand, a carrier-based PWM (CBPWM) algorithm was de-

veloped by T. Lee *et al.*¹¹ under SOC fault by transit- ing from three-level to two-level switching, thus keep the output voltage at the same rating value as the pre- fault condition. Despite the fact that two-level switch- ing leads to an increment of harmonic distortion in output voltages, the reliability of the VSI in certain safety-critical applications has a higher priority^{10,11}. Compared with other PWM techniques, for examples, space vector PWM (SVPWM), CBPWM is the highly popular algorithm which is based on the compar- ison of sinusoidal reference signals with carrier waves, thus make the modulation scheme easier to be imple- mented¹⁰. Thus, the implementation of CBPWM for 322-type VSI should be an attractive solution. There- fore, CBPWM algorithm will be developed in this pa- per. The main contents of this paper include three parts. Firstly, switching states and voltage vectors of the 322-type VSI are presented. Secondly, the princi- ples of the proposed 322-CBPWM techniques includ- ing 322-SPWM and 322-MOCBPWM techniques are analyzed. Finally, simulation in MATLAB/Simulink and experimental implementation are carried out, giving the results for discussion and evaluation.

SWITCHING STATES AND OUTPUT VOLTAGES OF 322-TYPE VSI

Switching States

Considering a 322-type VSI in Figure 1(c), the switch- ing states will be described as following:

$$\begin{cases} S_{A1} + S'_{A1} = 1 \\ S_{A2} + S'_{A2} = 1 \\ S_{B1} + S'_{B1} = 1 \\ S_{C1} + S'_{C1} = 1 \end{cases} \quad (1)$$

For convenience in analysis, the phase-leg switching states set $\{S_A, S_B, S_C\}$ is used, which is defined as:

$$\begin{cases} S_A = S_{A1} + S_{A2} \\ S_B = 2S_{B1} \\ S_C = 2S_{C1} \end{cases} \quad (2)$$

Where $0 \leq S_{A1} \leq S_{A2} \leq 1$, $0 \leq S_{B1} \leq 1$, and $0 \leq S_{C1} \leq 1$, respectively.

The synthesized voltage vector in the stationary α - β coordinate system corresponding to each switching set $\{S_A, S_B, S_C\}$ is defined as¹²:

$$\vec{V} = \frac{2}{3} (S_A + a.S_B + a^2.S_C) \cdot \frac{V_{dc}}{2} \quad (3)$$

where $a = e^{j2\pi/3}$. Table 1 lists available switching states of 322-type VSI and the corresponding synthe- sized output voltage vectors, which are then illustrated in Figure 2.

The space vector diagram has total of 12 vectors, which generate 11 different output voltages. There are 6 large vectors, named v14, v16, v18, v20, v22, and v24, respectively, which located at the large hexagon of 3L TNPC VSI. Each large vector has the magnitude of $(2/3)V_{dc}$. Two medium vectors are v17 and v23 which locate in the β -axis and have a magnitude of $(1/\sqrt{3})V_{dc}$. Two small vectors are v1 and v11 which locate at the small hexagon according to 2L VSI and in the α -axis, each has the magnitude of $(1/3)V_{dc}$.

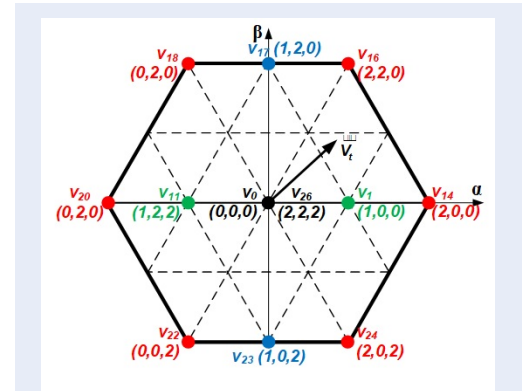


Figure 2: Space vector diagram of 322-type VSI.

Two zero vectors v_0 and v_{26} are both located at the hexagonal center.

Output voltages

The instantaneous phase-leg voltages are described by the following equations:

$$\begin{cases} V_{AO} = S_A \cdot V_{dc}/2 \\ V_{BO} = S_B \cdot V_{dc}/2 \\ V_{CO} = S_C \cdot V_{dc}/2 \end{cases} \quad (4)$$

The average value of each phase-leg voltage can be de- termined by the corresponding control voltage $\{v_{dkA}, v_{dkB}, v_{dkC}\}$, respectively:

$$\begin{cases} V_{AO} = v_{dkA} \cdot V_{dc}/2 \\ V_{BO} = v_{dkB} \cdot V_{dc}/2 \\ V_{CO} = v_{dkC} \cdot V_{dc}/2 \end{cases} \quad (5)$$

For them, the corresponding control voltages can be determined:

$$\begin{cases} v_{dkA} = \frac{V_{AO}}{V_{dc}/2} \\ v_{dkB} = \frac{V_{BO}}{V_{dc}/2} \\ v_{dkC} = \frac{V_{CO}}{V_{dc}/2} \end{cases} \quad (6)$$

Table 1: Switching States Of 322-type VSI

SA	SB	SC	Switching vectors	\vec{V}
0	0	0	v0 (0,0,0)	0
1	0	0	v1 (1,0,0)	$(1/3)V_{dc}$
1	2	2	v11 (1,2,2)	$-(1/3)V_{dc}$
2	0	0	v14 (2,0,0)	$(2/3)V_{dc}$
2	2	0	v16 (2,2,0)	$(1/3 + j/\sqrt{3})V_{dc}$
1	2	0	v17 (1,2,0)	$(j/\sqrt{3})V_{dc}$
0	2	0	v18 (0,2,0)	$(-1/3 + j/\sqrt{3})V_{dc}$
0	2	2	v20 (0,2,2)	$-(2/3)V_{dc}$
0	0	2	v22 (0,0,2)	$(-1/3 - j/\sqrt{3})V_{dc}$
1	0	2	v23 (1,0,2)	$-(j/\sqrt{3})V_{dc}$
2	0	2	v24 (2,0,2)	$(1/3 - j/\sqrt{3})V_{dc}$
2	2	2	v26 (2,2,2)	0

PROPOSED METHOD OF CARRIER-BASED PWM FOR 322-TYPE VSI (322-CBPWM)

Principle of 322-CBPWM

Considering a load voltage vector $\vec{V}_t = V_m e^{j\theta}$ where V_m is the voltage magnitude and θ is the phase angle, respectively, the principle of 322-CBPWM technique to synthesize \vec{V}_t includes two steps. The first one is determining three control voltages $\{v_{dkA}, v_{dkB}, v_{dkC}\}$. The second one uses these signals to implement carrier wave techniques, thus determining the switching states for each switch of the 322-type VSI.

Voltage modeling of inverter

Three-phase load voltages can be defined as:

$$\begin{cases} v_{tA} = V_m \cos q \\ v_{tB} = V_m \cos(q - 2p/3) \\ v_{tC} = V_m \cos(q + 2p/3) \end{cases} \quad (7)$$

The analysis of 322-CBPWM is achieved by an average voltage model, as shown in Figure 3.

$$\begin{cases} V_{AO} = V_{tA} + V_{off} \\ V_{BO} = V_{tB} + V_{off} \\ V_{CO} = V_{tC} + V_{off} \end{cases} \quad (8)$$

In general, the offset voltage value is in a range between two limitations, the minimum value V_{offmin} and the maximum value V_{offmax} , respectively:

$$V_{offmin} \leq V_{off} \leq V_{offmax} \quad (9)$$

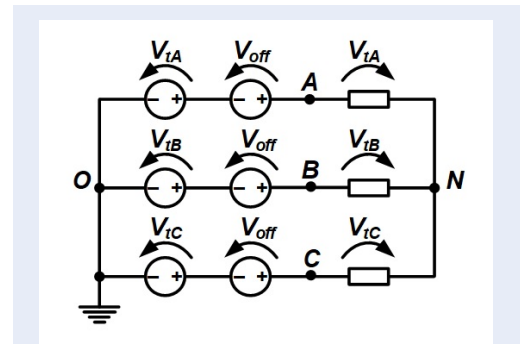


Figure 3: Average voltage model.

From load phase voltages calculated in (6), their maximum and minimum values can be obtained:

$$\begin{cases} max = \max(V_{tA}, V_{tB}, V_{tC}) \\ min = \min(V_{tA}, V_{tB}, V_{tC}) \end{cases} \quad (10)$$

Based on *max* and *min* values, values of V_{offmax} and V_{offmin} are determined:

$$\begin{cases} V_{offmax} = V_{dc} - max \\ V_{offmin} = -min \end{cases} \quad (11)$$

Various modulation techniques can be proposed depending on the selected V_{off} . In 322-sinusoidal PWM (322-SPWM) technique, V_{off} is determined by the following expression:

$$V_{off} = V_{dc}/2 \quad (12)$$

In medium offset 322-CBPWM (322-MOCBPWM) technique, the value of V_{off} is determined by:

$$V_{off} = (V_{offmax} + V_{offmin}) / 2 \quad (13)$$

From load phase voltages $\{V_{tA}, V_{tB}, V_{tC}\}$ in (8) and offset voltage V_{off} in (12) or (13), three control signals $\{v_{dkA}, v_{dkB}, v_{dkC}\}$ can be determined by (6).

Carrier-based implementation

In this step, three control voltages are compared with the corresponding triangular-form carrier waves. Due to the reason that SOC fault occurs on the neutral-point-connected legs of phase B and C, the carrier waves of these phases must be changed to two-level mode whereas phase A still works in three-level mode. Therefore, there are two carrier waveforms needed for phase A, which are v_{car1} with the magnitude between 1 and 2, and v_{car2} with the magnitude between 0 and 1, respectively. For the phase-leg B and C, there is only one carrier wave v_{car} needed with the magnitude between 0 and 2.

The switching states and modulating signals are described in the following expressions:

$$\begin{aligned} 0 \leq v_{dkA} \leq v_{car2} \leq 1 : S_{A1} = 0; S_{A2} = 0 \\ 0 \leq v_{car2} \leq v_{dkA} \leq 1 : S_{A1} = 0; S_{A2} = 1 \end{aligned} \quad (14)$$

$$\begin{aligned} 1 \leq v_{dkA} \leq v_{car1} \leq 2 : S_{A1} = 0; S_{A2} = 1 \\ 1 \leq v_{car1} \leq v_{dkA} \leq 2 : S_{A1} = 1; S_{A2} = 1 \end{aligned} \quad (15)$$

$$\begin{aligned} 0 \leq v_{dkB} \leq v_{car} \leq 2 : S_{B1} = 0; \\ 0 \leq v_{car} \leq v_{dkB} \leq 2 : S_{B1} = 1; \end{aligned} \quad (16)$$

$$\begin{aligned} 0 \leq v_{dkC} \leq v_{car} \leq 2 : S_{C1} = 0; \\ 0 \leq v_{car} \leq v_{dkC} \leq 2 : S_{C1} = 1; \end{aligned} \quad (17)$$

The switching states of each switch and instantaneous output phase-leg voltages of 322-type VSI in one sampling carrier cycle are illustrated in Figure 4. The algorithm in the proposed 322-SPWM and 322-MOCBPWM techniques is illustrated in Figure 5.

Modulation index definition

In this study, the modulation index is defined by the following expression:

$$m = \frac{V_{t(1)}}{V_{dc}/\sqrt{3}} \quad (18)$$

where $V_{t(1)}$ is the fundamental magnitude of phase load voltage, and $V_{dc}/\sqrt{3}$ is the maximum fundamental magnitude of phase load voltage. In linear modulation, the limit of modulation index is $0 \leq m \leq 0.866$ for 322-SPWM and $0 \leq m \leq 1$ for 322-MOCBPWM, respectively.

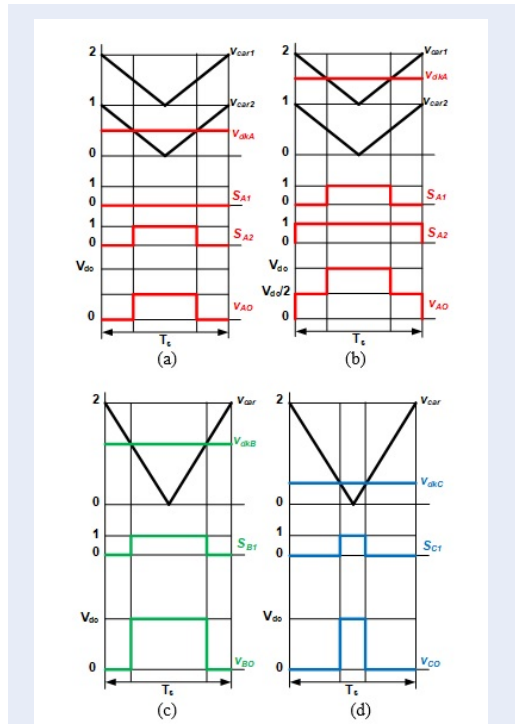


Figure 4: Switching states and output phase-leg voltages of 322-type VSI: (a) Phase A with $0 \leq v_{dkA} \leq 1$; (b) Phase A with $1 \leq v_{dkA} \leq 2$; (c) Phase B; (d) Phase C

Total harmonic distortion and weighted-total harmonic distortion definitions

The Fourier series of a given periodical voltage $v(t)$ can be written as follows:

$$v(t) = V_{(0)} + \sum_{n=1}^{\infty} V_{(n)} \cos(n\omega t) \quad (19)$$

where $V_{(0)}$ is the magnitude of zero-order component, or DC component of the voltage $v(t)$. The second term in (20) denotes the sum of sinusoidal components at various higher frequencies where n is the order of harmonic component. For instance, $n=1$ corresponding to the fundamental component (50 Hz) while $n=3$ is the third harmonic component (150 Hz), respectively.

Total harmonic distortion (THD) is usually used to evaluate the quality of a periodical signal. Its definition is¹³:

$$THD(v) = \frac{\sqrt{\sum_{n=2}^{\infty} V_{(n)}^2}}{V_{(1)}} \quad (20)$$

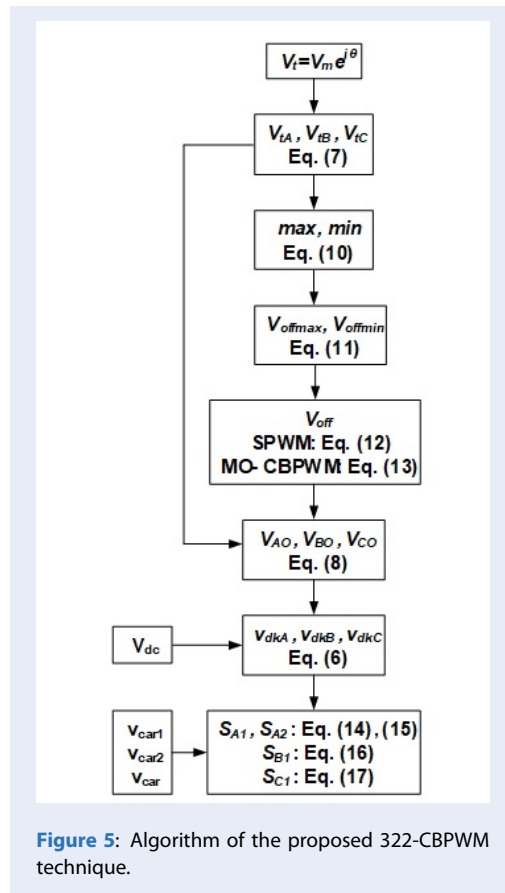


Figure 5: Algorithm of the proposed 322-CBPWM technique.

The weighted-total harmonic distortion (WTHD) is defined by the following equation¹³:

$$WTHD(v) = \frac{\sqrt{\sum_{n=2}^{\infty} (V_n/n)^2}}{V_{(1)}} \quad (21)$$

where $V_{(1)}$ is the magnitude of fundamental component of $v(t)$.

RESULTS AND DISCUSSIONS

Two proposed techniques, *i.e.* 322-SPWM and 322-MOCBPWM, are firstly simulated by a MATLAB/Simulink model as shown in Figure 6, and secondly implemented on an experiment setup, as shown in Figure 7. Control card TI TMSF28377D is used as the main controller while the 322-type VSI is built from IGBTs STGW40N120KD and diodes STTH3012. Voltages and currents waveforms are measured by the digital oscilloscope Tektronix TDS 2024C. The simulation and experimental parameters are listed in Table 2.

Simulation and experiment results of 322-SPWM technique are presented in figures from Figure 8 to

Table 2: Simulation And Experimental Parameters

DC-link voltage	100	[V]
Load resistance	16	[Ω]
Load inductance	60	[mH]
Carrier frequency	5	[kHz]
Dead-time (in experiment)	2	[μs]

Figure 12 while those of 322-MOCBPWM technique are illustrated in Figure 13 to Figure 17.

Figure 8 shows the simulated output voltages and currents of 333-type VSI under different operating modes while Figure 9 shows the experiment results of output signals in the 322-type VSI working with the proposed 322-SPWM algorithm. The simulated spectrum analysis results of voltages are presented in Figure 10.

It is clear that under simultaneous SOC fault on phase B and phase C which makes the 333-type VSI become a 322-type one, there are not only distorted output voltages v_{AB} , v_{BC} , and v_{CA} but also distorted and unbalanced currents i_A , i_B , and i_C as shown in Figure 8(b). However, the proposed 322-SPWM technique improves voltages and current waveforms as shown in Figure 8(c).

Experiment results in Figure 9 show the effectiveness of 322-SPWM. However, there are some differences between the experiment values compared to simulation ones. As an example, with the proposed 322-SPWM, THD(v_{A3B2}) in simulation is 42.5% obtained from Figure 10(c) while the corresponding experiment value is 47.0% as shown in Figure 9(a). In terms of WTHD value, the experiment one is higher than that in simulation (0.88% compared to 0.37%).

The effectiveness of the proposed technique in simulation can be obtained from the spectrum analysis results in Figure 10. For instance, in terms of v_{AB} , in normal condition (333-type VSI with conventional SPWM or 333-SPWM), Figure 10(a) gives the results that THD(v_{A3B3})=24.5% while under faulty condition (322-type VSI with conventional PWM), the result THD(v_{A3B2_0})=68.9% is obtained from Figure 10(b). This THD value is as higher as 2.8 times compared with the first one. The WTHD value also rises significantly from WTHD(v_{A3B3})=0.20% to WTHD(v_{A3B2_0})=8.61%. The fundamental component magnitude of v_{AB} decreases badly from $V_{A3B3(1)}$ =80 V to $V_{A3B2_0(1)}$ =61.4 V, leads to a reduction of 23%. When applying the compensating PWM algorithm, the proposed 322-SPWM technique can recover the fundamental component voltage to the initial value, *i.e.*, 80 V, as shown in Figure 10(c).

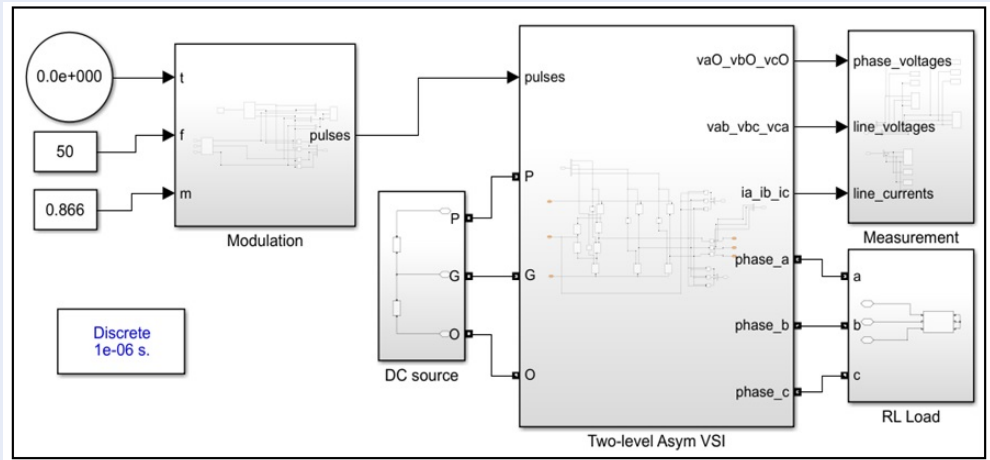


Figure 6: MATLAB/Simulink model.

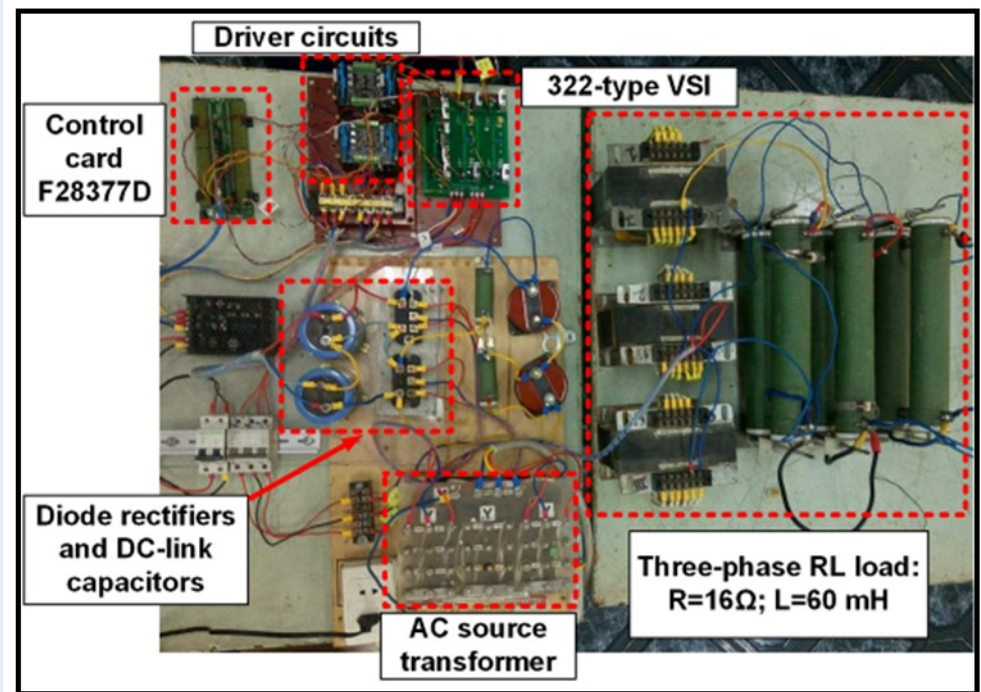


Figure 7: Experiment setup.

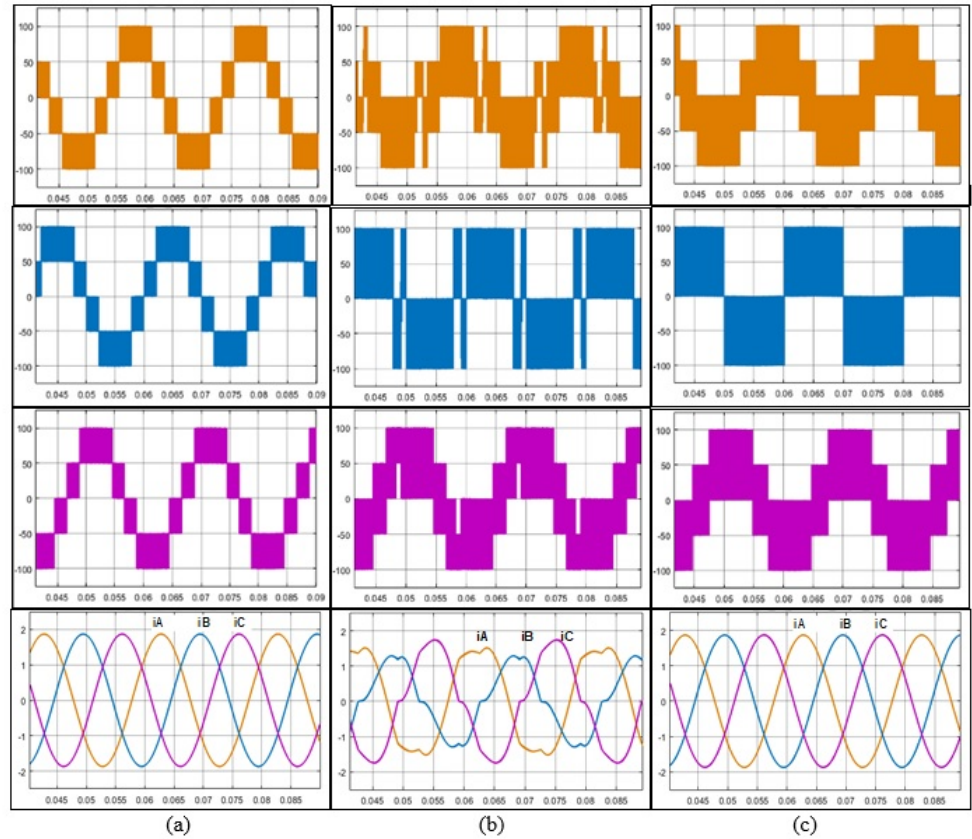


Figure 8: Simulated waveforms of output L2L voltages and currents in SPWM ($m=0.8$): (a) in pre-fault operation with conventional SPWM (333-SPWM); (b) in faulty operation with conventional SPWM; (c) in faulty operation with proposed 322-SPWM. From top to bottom: v_{AB} , v_{BC} , v_{CA} , and i_{ABC} .

In addition, the THD and WTHD values are also improved: Figure 10(c) shows that $THD(v_{A3B2})=42.5\%$ and $WTHD(v_{A3B2})=0.37\%$ while those are 68.9% and 8.61%, respectively, in the faulty condition. It is also seen that $THD(v_{A3B2})$ is higher than $THD(v_{A3B3})$ by 73% and $WTHD(v_{A3B2})$ is higher than $WTHD(v_{A3B3})$ by 85%.

Due to the fact that in the 322-type VSI, both L2L voltages v_{AB} and v_{CA} are measured between a 3L phase-leg and a 2L phase-leg, the effectiveness of proposed 322-SPWM technique in improvement harmonics distortion of v_{CA} are the same as those of v_{AB} . However, the L2L voltage v_{BC} is the worst case under SOC fault condition. Spectrum analysis in Figure 10(b) shows that under faulty condition, the fundamental magnitude value $V_{B2C2_0}=55.7$ V, causing a reduction of 30% compared with that in pre-fault operation. The harmonic distortion metrics are $THD(v_{B2C2_0})=83.0\%$ and $WTHD(v_{B2C2_0})=7.54\%$ while those values corresponding to normal operation

are $THD(v_{B3C3})=24.5\%$ and $WTHD(v_{B3C3})=0.20\%$, respectively, as shown in Figure 10(a). The proposed 322-SPWM technique provides not only the fundamental component of 80 V as same as pre-fault condition, but also the reduced THD and WTHD values, i.e., $THD(v_{B2C2})=50.1\%$ and $WTHD(v_{B2C2})=0.45\%$, respectively. As results, compared with the conventional PWM technique in faulty condition, the proposed technique advantageously reduce the harmonic distortion by 40% in terms of THD and by 94% in terms of WTHD, respectively.

The simulated THD and WTHD characteristics of output voltages in SPWM technique under different operations are shown in Figure 11 and Figure 12, respectively. From Figure 11 and Figure 12, it can be seen that the aforementioned faulty condition leads to a considerably increasing in harmonic content of v_{BC} compared with those of v_{AB} and v_{CA} , especially at low modulation indices. For instance, under normal operation with conventional PWM at $m=0.5$, the THD

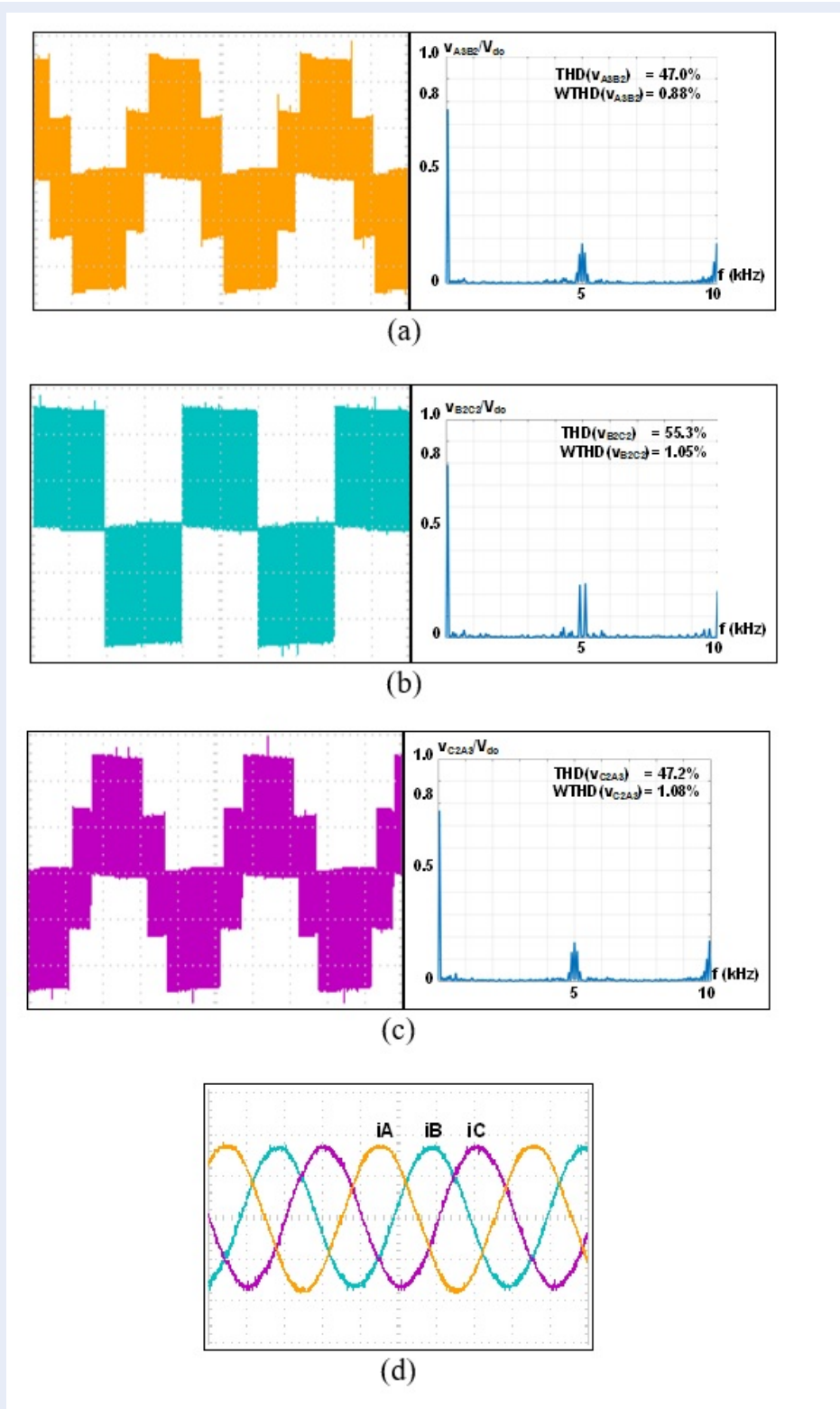


Figure 9: Experimented waveforms and spectra of output L2L voltages and currents of the 322-type VSI with the proposed 322-SPWM ($m=0.8$): (a) v_{AB} , (b) v_{BC} , (c) v_{CA} , (d) i_{ABC} . X-axis: 5 ms/div; Y-axis: 40 V/div (voltages), 1 A/div (currents)

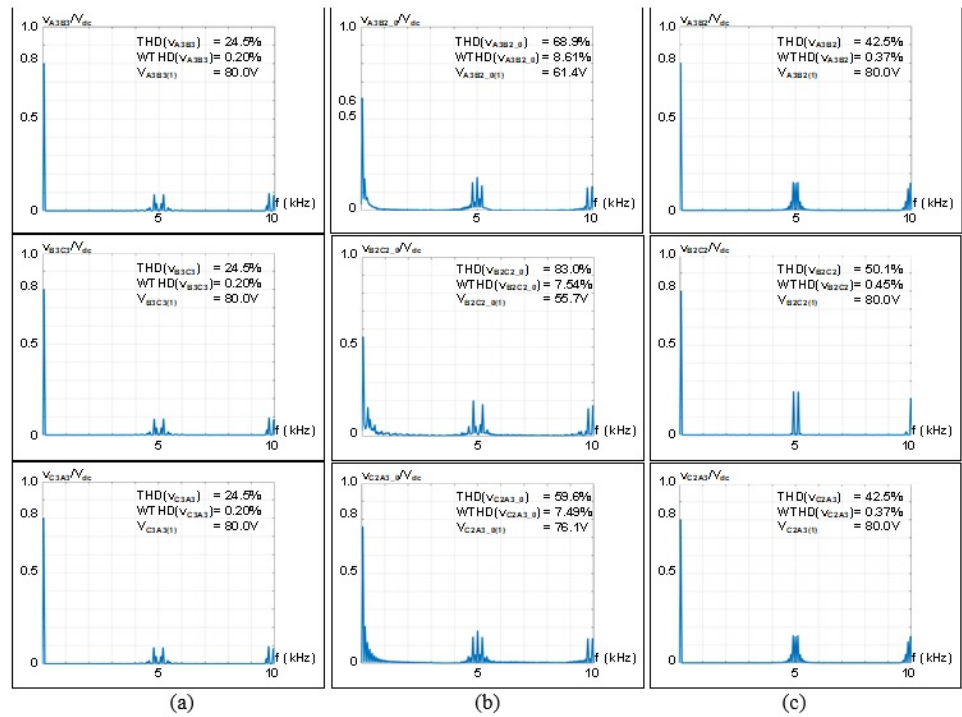


Figure 10: Simulated spectra of output L2L voltages in SPWM ($m=0.8$): (a) in pre-fault operation with conventional SPWM (333-SPWM); (b) in faulty operation with conventional SPWM; (c) in faulty operation with proposed 322-SPWM. From top to bottom: v_{AB} , v_{BC} , and v_{CA} .

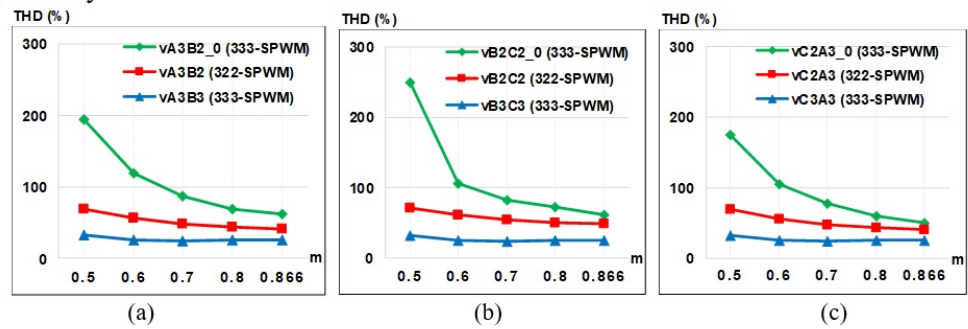


Figure 11: Simulated THD characteristics of output L2L voltages in SPWM technique: (a) v_{AB} ; (b) v_{BC} ; (c) v_{CA}

value of three L2L voltages, i.e., v_{A3B3} , v_{B3C3} , and v_{C3A3} are the same, at 32%, while under SOC faults with conventional PWM, these values obtained from Figure 11(b) are 194%, 250%, and 170%, respectively. In terms of WTHD, the normal operation values of three L2L voltages are the same, at 0.31% yet under faulty condition, these values are 15.9%, 34.9%, and 15.7%, respectively, are obtained from Figure 12(b). However, with the proposed 322-SPWM technique

implemented on the VSI under faulty condition, the harmonic distortion of three output voltages v_{A3B2} , v_{B2C2} , and v_{C2A3} shown in Figure 11(c) are improved to 69%, 71%, and 64% in terms of THD while the corresponding WTHDs are 0.59%, 0.44%, and 0.59%, respectively, as regards to $m=0.5$, as shown in Figure 12(c).

Simulation and experiment results of output L2L voltages and currents in the proposed 322-MOCBPWM

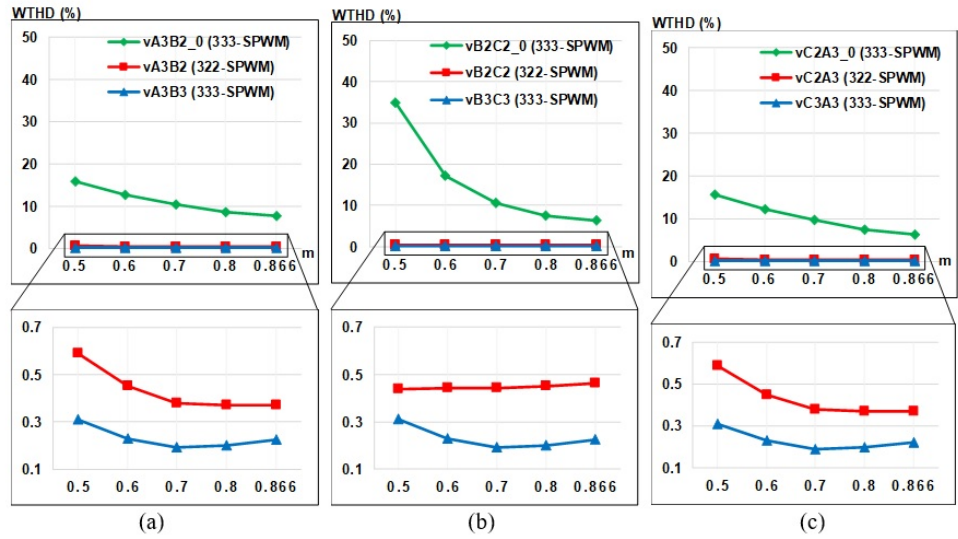


Figure 12: Simulated WTHD characteristics of output L2L voltages in SPWM technique: (a) v_{AB} ; (b) v_{BC} ; (c) v_{CA}

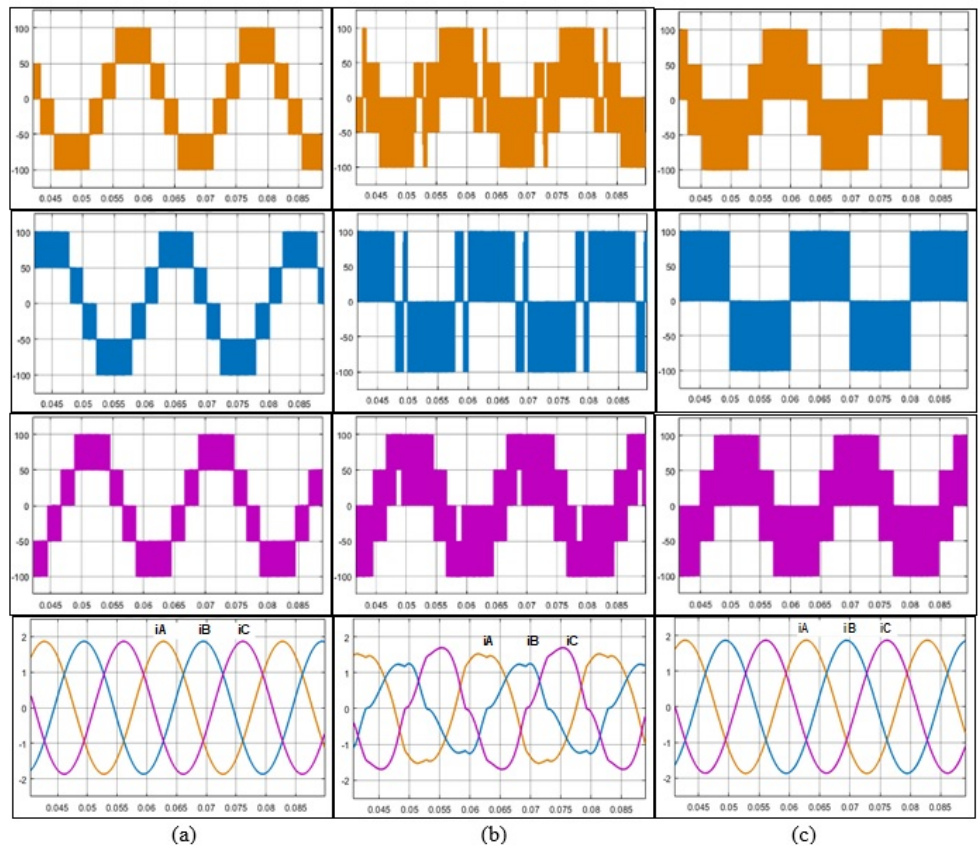


Figure 13: Simulated waveforms of output L2L voltages and currents in MOCBPWM ($m=0.8$): (a) in pre-fault operation with conventional MOCBPWM (333-MOCBPWM); (b) in faulty operation with conventional MOCBPWM; (c) in faulty operation with proposed 322-MOCBPWM. From top to bottom: v_{AB} , v_{BC} , v_{CA} , and i_{ABC} .

technique are illustrated in the following figures from Figure 13 to Figure 17. The waveforms of output voltages and currents in Figure 13 corresponding to MOCBPWM technique are similar to those of SPWM technique shown in Figure 8. The experiment results in Figure 14 verify the simulation ones. In the simulation, THD and WTHD of v_{A3B2} are 36.4% and 0.28%, respectively while those in experiment are 37.1% and 0.57%, respectively.

Similarly, with the 322-MOCBPWM algorithm, output voltages and currents in 322-type VSI are improved, as shown in Figure 15. As an example for $m=0.8$, Figure 15(a) and Figure 15(b) show significant increasing in harmonic distortion factor of v_{AB} from $\text{THD}(v_{A3B3})=22.5\%$ to $\text{THD}(v_{A3B2_0})=63.1\%$, and from $\text{WTHD}(v_{A3B3})=0.14\%$ to $\text{WTHD}(v_{A3B2_0})=6.45\%$, respectively. However, results from Figure 15(c) show that the proposed 322-MOCBPWM technique reduces the THD and WTHD of v_{AB} to 36.4% and 0.28%, respectively, i.e. a reduction of 42% as regards to THD and 96% as regards to WTHD. The fundamental voltage v_{AB} which reduced from 80 V in normal operation to 61.2 V in faulty operation with conventional MOCBPWM, as shown in Figure 15(a) and Figure 15(b), is now recovered to the initial reference value, i.e., $V_{A3B2(1)}=80$ V which shown in Figure 15(c). The effectiveness of 322-MOCBPWM technique on v_{BC} and v_{CA} can be observed in Figure 15, as well.

The simulated THD and WTHD characteristics of output voltages in MOCBPWM technique are illustrated in Figure 16 and Figure 17, respectively. Characteristics shown in Figure 16 and Figure 17 have the similarity to those in Figure 11 and Figure 12 so that the faulty operation of 333-type VSI leads to a considerably surge in harmonic distortion of L2L voltages, especially in the low values of modulation index. In addition, the voltage v_{BC} has the worst harmonic distortion compared to that of v_{AB} and v_{CA} , as regarding to the same value of m . For instance, under faulty condition for $m=0.5$, $\text{THD}(v_{B2C2_0})=285\%$ while $\text{THD}(v_{A3B2_0})=194\%$ and $\text{THD}(v_{C2A3_0})=170\%$. With use of the proposed 322-MOCBPWM technique, these values are 72%, 69%, and 64%, respectively. Therefore, there is only small difference between THD values of output voltages with the proposed algorithm. As regarding to WTHD factor, with use of compensating PWM algorithm, at $m=1$, they are $\text{WTHD}(v_{A3B2})=0.29\%$, $\text{WTHD}(v_{B2C2})=0.37\%$, and $\text{WTHD}(v_{C2A3})=0.37\%$ while those values under faulty condition are 4.30%, 4.13%, and 3.58%, respectively.

In terms of v_{BC} , simulated results in two CBPWM techniques with $m=0.8$ can be summarized by Table 3. Comparison between 322-SPWM technique and 322-MOCBPWM technique, it can be seen that the second one has the lower values of harmonic distortion factors. For instance, under faulty condition, the proposed 322-SPWM strategy has $\text{THD}(v_{B2C2})$ value of 50.1% while that of 322-MOCBPWM strategy is 45.7%. The corresponding $\text{WTHD}(v_{B2C2})$ of these algorithms are 0.45% and 0.36%, respectively. Hence, the harmonic distortion metrics of v_{BC} in 322-MOCBPWM are lower than that in 322-SPWM by 8.8% in terms of THD and by 20% in terms of WTHD, respectively.

CONCLUSION

This paper has presented the analysis and implementation of CBPWM techniques on a 333-type VSI working under simultaneous SOC faults on two neutral-point-connected phase-legs. Simulation results show that under the aforementioned SOC fault condition, the output voltages and currents are strongly distorted and unbalanced, with a reduction of fundamental voltages by up to 30%. The use of the proposed 322-SPWM and 322-MOCBPWM techniques can help attaining required fundamental voltages, and also lowering harmonic content after faulty condition. For the worst harmonic quality voltage v_{BC} , the proposed 322-SPWM has the ability in reduction of 40% and 94% in terms of THD and WTHD, respectively, while the corresponding results of 322-MOCBPWM technique are 42% and 96%, as regard to $m=0.8$. The advantages of 322-MOCBPWM technique compared to 322-SPWM technique are also presented, which are not only the extension of modulation range but also the better harmonic quality at the same operating condition. Compared with other studies cited, the proposed techniques do not need any additional hardware but still guarantees the desired values of fundamental voltages and balanced output currents. The proposed CBPWM algorithms are simple and easy for implementation, as well.

LIST OF ABBREVIATIONS

- CBPWM: Carrier-based pulse-width modulation
- SPWM: Sinusoidal pulse-width modulation
- MOCBPWM: Medium offset carrier-based pulse-width modulation
- VSI: Voltage source inverter
- SOC: Switch-open-circuit
- SSC: Switch-short-circuit
- THD: Total harmonic distortion
- UPS: Uninterruptible power supply

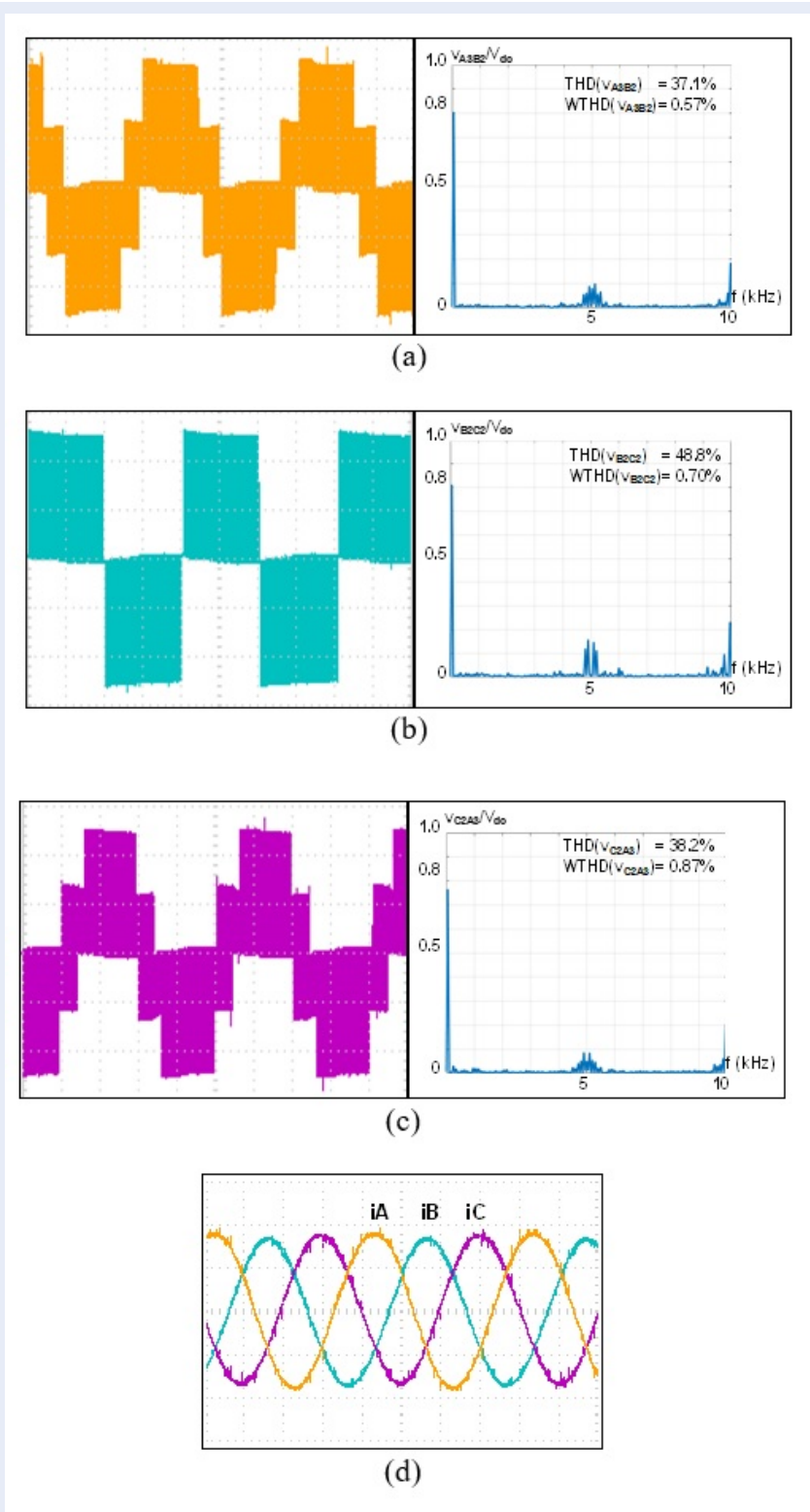


Figure 14: Experimented waveforms spectra of output L2L voltages and currents of the 322-type VSI with the proposed 322-MOCBPWM ($m=0.8$): (a) v_{AB} , (b) v_{BC} , (c) v_{CA} , and (d) i_{ABC} . X-axis: 5 ms/div; Y-axis: 40 V/div (voltages), 1 A/div (currents)

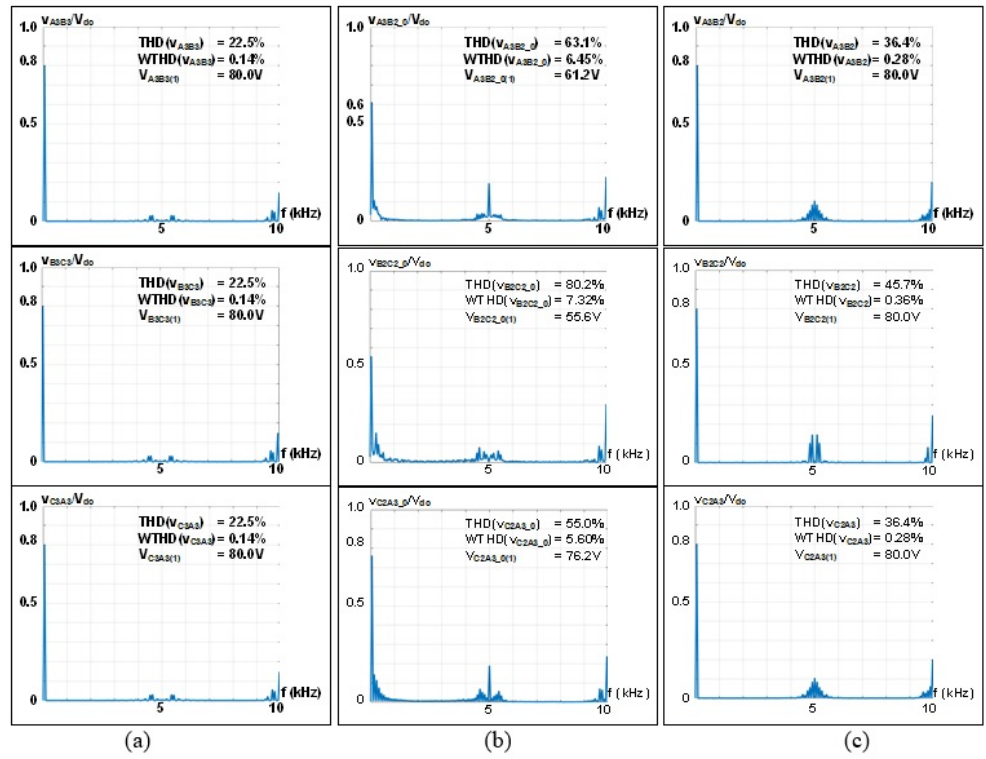


Figure 15: Simulated spectra of output L2L voltages in MOCBPWM ($m=0.8$): (a) in pre-fault operation with conventional MOCBPWM (333-MOCBPWM); (b) in faulty operation with conventional MOCBPWM; (c) in faulty operation with proposed 322-MOCBPWM. From top to bottom: v_{AB} , v_{BC} , and v_{CA} .

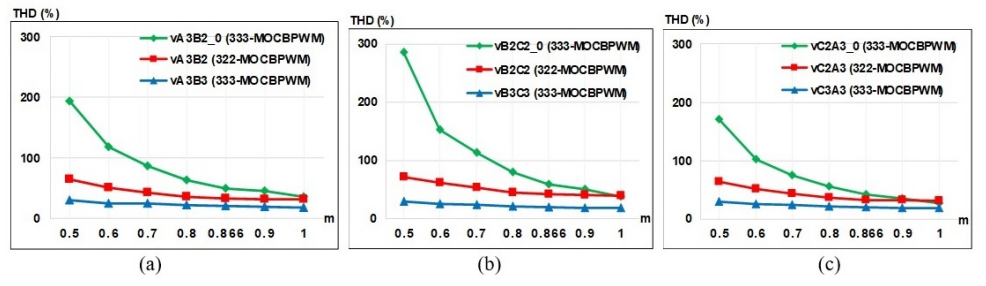


Figure 16: Simulated THD characteristics of output L2L voltages in MOCBPWM technique: (a) v_{AB} ; (b) v_{BC} ; (c) v_{CA}

Table 3: Simulated Harmonic Distortion Results Of V_{bc} ($M=0.8$)

Harmonic distortion metrics	Normal operation (with conventional PWM)		Faulty operation (with conventional PWM)		Faulty operation (with proposed PWM)	
	333-SPWM	333-MOCBPWM	333-SPWM	333-MOCBPWM	322-SPWM	322-MOCBPWM
THD (%)	24.5	22.5	83.0	80.2	50.1	45.7
WTHD (%)	0.20	0.14	7.54	7.32	0.45	0.36

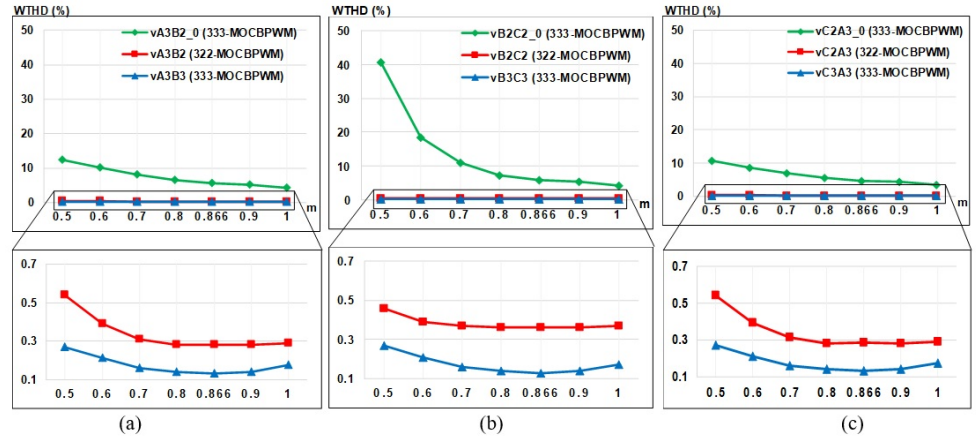


Figure 17: Simulated WTHD characteristics of output L2L voltages in MOCBPWM technique: (a) v_{AB} ; (b) v_{BC} ; (c) v_{CA}

PV: Photovoltaic

WTHD: Weighted-total harmonic distortion

2L VSI: Two-level voltage source inverter

322-type VSI: 322-type asymmetrical voltage source inverter

333-type VSI: Three-level T-type neutral-point clamped voltage source inverter

L2L: Line-to-line

CONFLICT OF INTERESTS

The author declares that there is no conflict of interests regarding the publication of this paper.

AUTHORS' CONTRIBUTIONS

Nho-Van Nguyen: Conceptualization, Methodology, Validation, Writing—review and editing, Supervision.

Phong Nguyen-Hong Le: Software, Validation, Data curation, Writing—original draft preparation.

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Nghiên cứu kỹ thuật điều chế độ rộng xung sóng mang cho mạch nghịch lưu nguồn áp 3 pha 3 bậc TNPC trong điều kiện hở mạch 2 nhánh nối điểm trung tính

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Bản quyền

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TÓM TẮT

Mạch nghịch lưu áp (VSI) đa bậc hiện được sử dụng rộng rãi nhờ vào những ưu điểm so với mạch 2 bậc truyền thống. Trong số các sơ đồ VSI, sơ đồ 3 bậc dạng diode kẹp hình T (3L TNPC VSI hay 333-type VSI) đang ngày càng nhận được sự quan tâm nghiên cứu. Do đặc điểm cấu trúc, mạch 333-type VSI có một số vấn đề về độ tin cậy khi vận hành, ví dụ như sự cố hở mạch khóa đóng ngắt (SOC) và sự cố ngắn mạch khóa đóng ngắt (SSC), các sự cố này làm giảm hiệu suất hệ thống, gây mất cân bằng và méo dạng điện áp và dòng điện ngõ ra, làm kích hoạt mạch bảo vệ. Trong một số ứng dụng, sự sụt giảm biên độ và méo dạng sóng hài trong điện áp ngõ ra dưới sự cố SOC là không được chấp nhận. Vì vậy, cần phát triển một kỹ thuật điều chế độ rộng xung (PWM) cho mạch 333-type VSI hoạt động trong điều kiện sự cố SOC để đảm bảo giá trị thành phần cơ bản của điện áp đầu ra theo yêu cầu. Sự cố SOC đồng thời trên 2 nhánh nối điểm trung tính của mạch 333-type VSI dẫn đến sự sụt giảm nghiêm trọng đối với điện áp đầu ra. Trong điều kiện này, mạch 333-type VSI trở thành mạch không đối xứng là 322-type VSI. Nhiều nghiên cứu khác nhau liên quan đến vận hành mạch 333-type VSI trong sự cố SOC đã được tiến hành. Tuy nhiên các nghiên cứu này đều sử dụng thêm linh kiện phần cứng để tạo thành một nhánh đóng ngắt bổ sung. Điều này làm tăng chi phí chế tạo và làm giảm hiệu suất của hệ thống do phát sinh thêm tổn hao. Trong bài báo này, hai kỹ thuật PWM sóng mang (CBPWM) được đề xuất cho mạch 322-type VSI, lần lượt là PWM dạng sin (322-SPWM) và CBPWM với hàm offset trung bình (322-MOCBPWM). Các kỹ thuật đề xuất được mô phỏng trước tiên bằng phần mềm MATLAB/Simulink và sau đó được triển khai trên phần cứng thực nghiệm. Chất lượng kỹ thuật đề xuất được đánh giá qua các chỉ số độ méo dạng sóng hài tổng (THD) và độ méo dạng sóng hài tổng có xét đến trọng số (WTHD) của điện áp ngõ ra. Kết quả mô phỏng cho thấy khi xét điện áp đầu ra vBC là điện áp bị ảnh hưởng nhiều nhất bởi sự cố, tại hệ số điều chế $m=0.8$ thông số THD và WTHD của kỹ thuật 322-SPWM được giảm với giá trị lần lượt là 40% và 94% so với trường hợp không áp dụng phương pháp đề xuất. Độ giảm tương ứng với kỹ thuật 322-MOCBPWM lần lượt là 42% và 96%. Các đặc tuyến THD và WTHD được trình bày nhằm xác minh tính hiệu quả của phương pháp đề xuất.

Từ khoá: mạch nghịch lưu nguồn áp, điều chế độ rộng xung sử dụng sóng mang, mạch nghịch lưu kẹp điểm trung tính kiểu T, sự cố hở mạch khóa đóng ngắt, độ méo dạng sóng hài tổng có xét đến trọng số

Trích dẫn bài báo này: Phong L N H, Nhờ N V. Nghiên cứu kỹ thuật điều chế độ rộng xung sóng mang cho mạch nghịch lưu nguồn áp 3 pha 3 bậc TNPC trong điều kiện hở mạch 2 nhánh nối điểm trung tính. *Sci. Tech. Dev. J. - Eng. Tech.*; 3(3):472-487.