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Research Article

Decentralized space vector pulse width modulation method for multilevel single-phase half bridge converters

Phu Cong Nguyen[1,2,3], Quoc Dung Phan[1,2,*], Dinh Tuyen Nguyen[1,2]

ABSTRACT

This study presents a space vector pulse width modulation (PWM) method for a multilevel single-phase decentralized power converter (DPC) called MSPDPC. The proposed model is built by connecting half-bridge cells in series. The output voltage can be adjusted according to demand by adding or subtracting cells. Cells use communication protocols to transmit and receive information with two neighboring cells. The received data contains information for the decentralized space vector pulse width modulation (DSVPWM) method proposed in this paper. In the proposed DSVPWM method, cells set up links to exchange information such as cell position, total cells in a phase, reference voltage amplitude, and reference frequency. The PWM control signals of each cell are calculated based on the information received. The study also focuses on evaluating the ability to adjust the switching vector and the corresponding dwell time of the cells when the structure of the DPC changes. The ability to dynamically reconfigure the DPC is a crucial feature that ensures uninterrupted power supply in case of one or several cell failures. The system automatically establishes a new state with the active cells. The proposed configuration and communication method between cells provide very fast configuration times. The load voltage of the DPC is adjusted to 0.5 times the voltage per cell, which allows the modulation voltage amplitude to be adjusted best according to the load requirements. The study used Matlab/Simulink software to review the initial assessments. The proposed model and algorithms are verified on the Digital Signal Processor (DSP) platform with a 220V/500W load.

Key words: multilevel/multiphase power converter, decentralized control, space vector pulse width modulation (SVPWM), dynamic reconfiguration, multicellular serial-parallel converters, half bridge converter

[1]*Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, Vietnam.*

[2]*Vietnam National University Ho Chi Minh City (VNU-HCM), Ho Chi Minh City, Vietnam.*

[3]*Department of Electrical and Electronics Engineering, Ho Chi Minh City University of Food Industry (HUFI), Ho Chi Minh City, Vietnam*

Correspondence

Quoc Dung Phan, Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, Vietnam.

Vietnam National University Ho Chi Minh City (VNU-HCM), Ho Chi Minh City, Vietnam.

Email: pqdung@hcmut.edu.vn

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1. INTRODUCTION

The modular structure is attracting the attention of researchers in the development trend of multilevel power converters [1,2]. The number of modules in series can be adjusted to reference the working characteristics and voltage quality criteria of the inverter. This includes the number of voltage levels supplied to the load, the switching voltages of the power transistors [3], and voltage distortion [4].

According to the conventional method, processing, calculation, and control of power converters are performed by a central controller [5,6]. The central processor is responsible for implementing algorithms such as controlling voltage between modules, controlling current between phases, reducing common mode voltage, and outputting appropriate PWM signals [2,7–9]. Therefore, it requires many connections to be established from the central controller to the modules. Each conventional microprocessor has limitations in terms of computing power, processing speed, and the number of input and output signal pins. As the demand for the number of power converter modules increases, processors become cumbersome, expensive, and complex, sometimes reducing operational reliability. To reduce dependence on the central controller, recent studies on multilevel power converters have announced a new approach to building decentralized power converters (DPCs) [10,11]. Depending on the application, control target, and structure of the DPCs, researchers have published three main content areas. The first content gathers studies on DPCs controlled as master-slave or central-local [10,12]. The power converter modules work independently of each other, generating appropriate PWM signals by analyzing the voltage and current of the module, which is the second content [13,14]. This research direction has the advantage of being completely dispersed; however, the control algorithm is complex and only suitable for some power converter structures. The third main content focuses on studying the structure of DPCs, where the modules perform information exchange with neighboring modules, and each module includes a microprocessor and

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a dynamic circuit [15–18].

The signal transmission between modules in DPCs can vary depending on the structure, control objective, and control method. Transmission can occur through amplitude [19] and phase angle of the carrier [20], module voltage [21], branch current [22], position of module [19], total modules [19], and more. This structure is suitable for the design of DPCs, making it compatible with a wide variety of power converter models. Power converters can easily add or remove several modules from the system, ensuring flexibility in operation and control, which is an outstanding feature of DPCs [23].

In modern power converters, it is common for the PWM signal to be modulated by two methods: CPWM [10–12] and SVPWM [1,2,6,24]. Recently, the CPWM method has been published in some studies on DPCs for the models of cells connected in series [19], in parallel [22], and in series and parallel [25]. The main topics of the CPWM method have been addressed, including carrier phase shift control for flying capacitor converters [21], carrier level shift control for half bridge and full bridge models [19,26], and carrier phase shift control for half bridge cells connected in parallel [19,22]. However, the use of SVPWM for DPCs has not been fully studied and published. Studies [23,27] have presented the structure and SVPWM method for DPC using full bridge cells connected in series. Research [27] presents multilevel and multiphase DPC, with initial research results showing that the control algorithm for cells is quite complex. Meanwhile, the study [23] presented the SVPWM method for MSPDPC using full bridge cells connected in series. By using the full bridge inverter model, when one cell is removed or added to the DPC, the level of the variable load voltage is increased or decreased by two, ensuring that the number of levels is always odd and the maximum output voltage amplitude is increased or decreased by one cell voltage.

As for the half bridge inverter model shown in Figure 1, when removing or adding one cell to the system, the number of output voltage levels increases by one, and the output voltage increases or decreases by a half cell voltage. Therefore, DPCs can easily, appropriately, and accurately adjust voltage according to the output voltage needs of the load when using a half-bridge cell structure. However, the SVPWM method for MSPDPC using the half bridge module has not been studied and published yet.

The time it takes for a DPC system to reach steady state during startup and configuration changes is one of the important issues to consider. The control structure and method presented in studies [19,26] have very fast configuration times. This is accomplished through the exchange of position signals from the previous cell and data on the total cells in the converter. The implementation method is quite simple, effective, and highly reliable. The control algorithm [26] allows DPCs to operate with only one cell, while other algorithms require a minimum of three cells in the system to function [26]. In the experimental results of the study [19], information exchange between cells is done using DAC, ADC, and GPIO signal pins. However, if the number of cells in the DPCs is increased, this could become a limitation.

This study presents the structure of a single-phase multi-level DPC using SVPWM. The proposed model is implemented by connecting half-bridge cells to each other. The PWM control signal of the cells is calculated using the cell position signal and the number of cells in the system. The study uses Serial Communications Interfaces (SCI) to reduce the impact of interference on transmission and reception of control voltage frequency, amplitude, cell position, and total cells. When SCI is used in DPC, it becomes easier to increase the number of cells in DPCs. This study also improves the method of transmitting total cell information in the system compared to research [19].

This improvement is suitable for SCI implementations that will be applied to the DSVPWM converter. The research focuses on evaluating the responsiveness of the load voltage according to the control voltage, the ability to dynamically reconfigure when it is necessary to add or remove some cells, and the adjustment of the output voltage amplitude in multiples of a half cell voltage. The proposed DSVPWM structure and method ensure the ability to operate even in the case of only one cell in the system. The proposals will be verified through simulations and experimental results.

2. THE SVPWM METHOD FOR MULTILEVEL SINGLE-PHASE HALF BRIDGE CONVERTER

In 2-, 3-, and 4-level converters, the voltage space vectors (VSV) are arranged as shown in Figure 2. The supply voltage of each cell is Vdc, where P, N, and 0 represent the positive, negative, and zero vectors, respectively. The reference voltage is formulated as shown in Equation (1).

$$v_r = V_m \sin(\omega t) \quad (1)$$

where V_m, ω are the peak amplitude and angular frequency of the reference voltage, t is time variable.

The fixed vector v_1 and the rotating vector v_2 can be determined from the v_r vector. The v_{ref} vector is created by projecting the v_r vector onto the α axis. The switching pulse is determined based on the 2 nearest vector principle. The v_{ref} vector is then used to determine the instantaneous voltage amplitude across the load. Figure 2a shows the arrangement of VSV for a 4-level inverter system with 3 active cells. The four operating states of the four-level converter are $3/2V_{dc}$, $-1/2V_{dc}$, $1/2V_{dc}$, and $3/2V_{dc}$. Therefore, the proposed four-level inverter has three modulation zones: $\{-3/2V_{dc}, -1/2V_{dc}\}$, $\{-1/2V_{dc}, 1/2V_{dc}\}$, and $\{1/2V_{dc}, 3/2V_{dc}\}$. Depending on the frequency of the modulation voltage, the v_{ref} vector moves between the three active zones. The diagram for the VSV of a three-level inverter is shown in Figure 2b. The three-level single-phase inverter consists of two cells. The three operating states of the three-level converter are $-V_{dc}$, $0V_{dc}$, and V_{dc}. Two of the three states represent the active state, while the remaining one represents the zero phasor positioned at the center of the plane. The zero vector will appear in switched states if the total number of cells is even. The total number of cells, denoted by N_{total}, is the total cells in multilevel single-phase power converter by concatenating half bridge cells in series. The number of levels, denoted by $n_{l,}$ is equal to the total number of cells N_{total} plus 1, as shown in (2). The voltage between two adjacent levels is $0.5V_{dc}$.

$$n_l = N_{total} + 1 \tag{2}$$

As shown in Figure 2a and Figure 2b, assuming the reference voltage v_r has peak amplitude of $0.7V_{dc}$, the reference voltage is still within the modulation zones of the system that has 2 or 3 cells. However, there is a difference in the number of switching states when performing SVPWM. If the inverter has 3 cells, then there are four switching states. Meanwhile, the number switching states is 2 if power converter has 2 cells in a phase. Therefore, a general algorithm for the multilevel modulation technique is proposed; the modulation voltage is an integer multiple of the supply V_{dc} voltage plus a parameter l as shown in (3). The process of calculating the PWM control signals is done by the proposed algorithm, as shown in (1), (3)-(5).

$$a_r = \frac{v_r}{V_{dc}} + l \tag{3}$$

where:

+ l = 0 if the total number of cells in the power converter is even, then the modulation voltage level is odd.

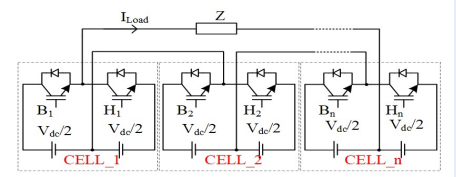

Figure 1: Multicellular single-phase half bridge converter

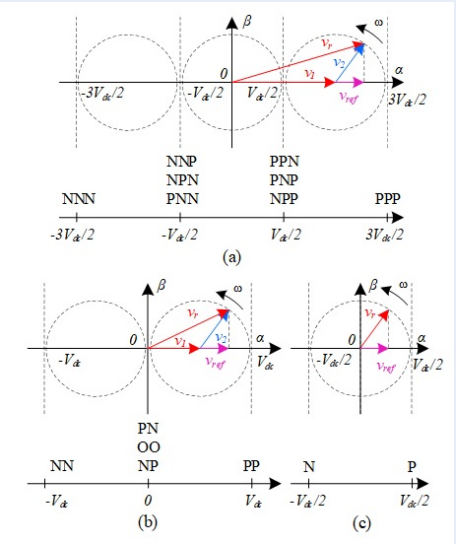

Figure 2: . Principle of SVPWM for multi-level single-phase converter. (a) 4 level. (b) 3 level. (c) 2 level

+ l = 0.5 if the total number of cells in the power converter is odd, then the modulation voltage level is even.

The switching vector has the form as shown in (4):

$$a_i = floor(a_r) \tag{4}$$

In equation (4), the operator *floor(x)* is used, which rounds each element of x to the nearest integer less than or equal to that element.

The switching time is shown in (5).

$$\begin{cases} t_1 = a_r - a_i \\ t_2 = 1 - t_1 \end{cases} \tag{5}$$

Based on the inverter model, the central processor generates the required PWM signals to control the corresponding modules. If the inverters use a centralized controller, the selection of switching vectors for the cells is predetermined and fixed during operation. However, for the inverter that needs to automatically reconfigure as cells are added or removed,

the central processor needs to establish new connection and redefine the PWM control signals for each cell. This process requires the system to be stopped, and the inverter need to be adjusted before returning to operation. Therefore, there is an urgent need to design a MSPDPC system that can dynamically reconfigure cells without requiring the system to stop.

3. PROPOSED SVPWM METHOD FOR MSPDPC

The control connection diagram for MSPDPC is presented in Figure 3. The control structure uses the ordinal numbering method to determine the cell position and total number of cells in the system. The cell position is defined as follows: at time step k, the position data of cell_n will be incremented by one from the data received by cell_n-1 (*count_in*) and defined as *count_out*. All active cells in the inverter use the same control algorithm. The first cell has a value of 0. The value of final cell position is considered to be the total active cells in the inverter and it is transmitted through active cells in the MSPDPC. In the study[26], the total number of cells will be transmitted from the last cell to the first cell and continue to pass through all the remaining cells in turn. In this paper, another approach is proposed to pass the total number of cells signal to the cells in the system, then the last cell will transmit the total cells from the last cell to cell_n-1 and transmit through all cells in turn until the first cell in the system. This proposal would be suitable in the use of SCI in DPC.

The cell position is determined by equation (6).

$$i_n^k = count\_in_n^k \tag{6}$$

where k is the time step.

The total cells in the inverter are determined by equation (7).

$$N_{total}^k = number\_in_n^k \tag{7}$$

The outstanding advantage of the SVPWM method for DPCs is its ability to automatically adjust the switching vector and appropriate switching time for each cell. In DPCs, the cells operate independently of one another. The algorithm to determine the switching vectors and dwell time at the vertex of the vector is proposed in equations (8)-(9). For better explanation, let's consider a DPC with 3 or 4 half-bridge cells with a reference voltage of $1.2V_{dc}$ and a reference frequency of 50Hz, as illustrated in Figure 4, which shows the a_i and a_s vectors in the case of a system with 4 cells or 3 cells. The conversion of the a_i vector to the a_s vector is achieved using equations (8). The objective of this conversion is to obtain the as vector between 0 and N_{total}-1. This enables the switching vector of the cell to be determined using equation (9).

$$a_s^k = a_i^k + fix\left(\frac{N_{total}^k}{2}\right) \tag{8}$$

where operator *fix(x)* rounds each element of x to the nearest integer toward zero.

$$a_{sn}^k = i_n^k \tag{9}$$

The implementation algorithm of one cell is detailed in Figure 5. The relationship between the total active cells and the modulation voltage is bound by equation (10).

$$V_{max}^k = \frac{N_{total}^k}{2} V_{dc} \tag{10}$$

In MSPDPC, all activated cells have similar roles and tasks: generating switching vectors and appropriate switching times based on the reference voltage. Any cell in the DPC can be used as the master cell; typically, cell_1 is selected as the master cell. The task of the master cell is to provide the reference voltage for all active cells in the DPC, including itself. At cells, the reference voltage is synthesized using equation (1), and appropriate switching vectors and switching times are generated using equations (3)-(9).

4. SIMULATION RESULTS

To evaluate the proposed algorithm, the DPC model as shown in Figure 1 and Figure 3 are simulated on Matlab/Simulink software. The inverter consists of 4 cells half bridge connected in series. The functions and tasks of the inputs and outputs in one cell are described in Table 1. Load parameters, direct current (DC) voltage sources of cells, sampling time and switching frequency are presented in Table 2.

Each cell uses two DC voltage sources of 40V, so the supply voltage for each cell is 80V. All cells in the inverter are active, and the output voltage have 5 levels. The output voltage is synthesized by 4 cells. The response of the output voltage and load current for a stepwise change of the modulation index and total number of cells in the inverter are shown in Figure 6. Throughout the evaluation process, the modulation frequency is 50Hz. When DPC starts, the modulation index (*M*) is 0.9375, the output voltage has 5 levels: 160V, 80V, 0V, -80V, -160V. At 0.02 seconds, M is 0.375, and the output voltage has 3 levels: 80V, 0V, -80V. The output voltage is synthesized by cell_1 and cell_2. At 0.06 seconds, cell_3 is removed. The system has 3 cells left, and the output voltage has 4 levels:

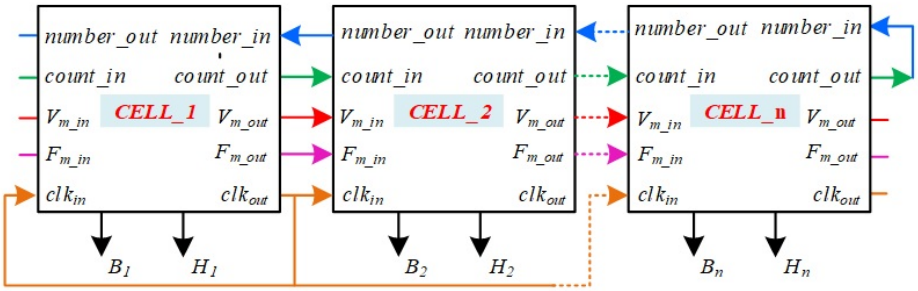

Figure 3: Communication between cells in the system

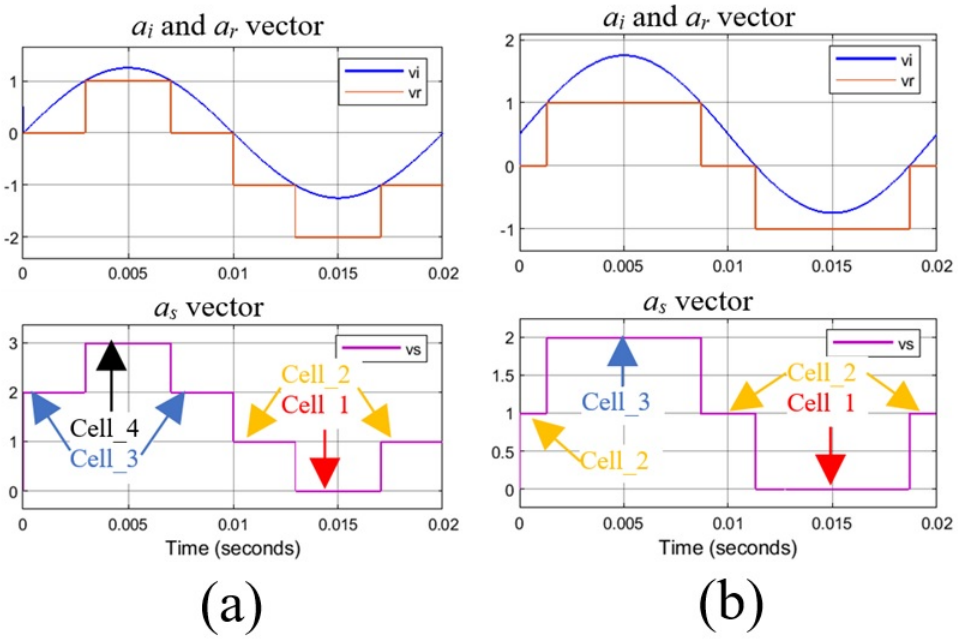

Figure 4: v_r and v_i vector. (a) 4-cells system (b) 3-cells system

120V, 40V, -40V, -120V. At 0.1 seconds, cell_4 is removed, and DPC has cell_1 and cell_2 left. The output voltage has 3 levels: 80V, 0V, -80V. At 0.14 seconds, cell_3 and cell_4 is reinserted, and the output voltage has 3 levels: 80V, 0V, -80V. Finally, at 0.18 seconds, M is 0.9375, and the output voltage of DPC has 5 levels. If the reference voltage is still less than the maximum voltage that the cells can be modulated, the number of levels of output voltage depends on the number of active cells. Indeed, during the simulation from 0.02 to 0.18 seconds, the peak amplitude of the reference voltage is fixed at 60V. To modulate the output voltage of 60V, the system needs the voltage contribution of 2 or 3 cells. Observed from time 0.06 to 0.1 seconds, the system has 3 cells, the output voltage has 4 levels. Observed from 0.02 to 0.06 seconds and 0.1 to 0.18 seconds, the total number of cells in the system is even, and the output voltage has 3 levels. Thus, the simulation results are consistent with the proposed algorithm.

In the case of a dynamically reconfigured system, the response of the output voltage and load current is shown in Figure 7. At the time of start-up, the system has all 4 active cells, and the output voltage has 5 levels, which is synthesized by 4 cells. At 0.04 seconds, cell_3 and cell_4 are removed. The system has 2 cells left, and the output voltage has 3 levels, which is synthesized by cell_1 and cell_2. At 0.08 seconds,

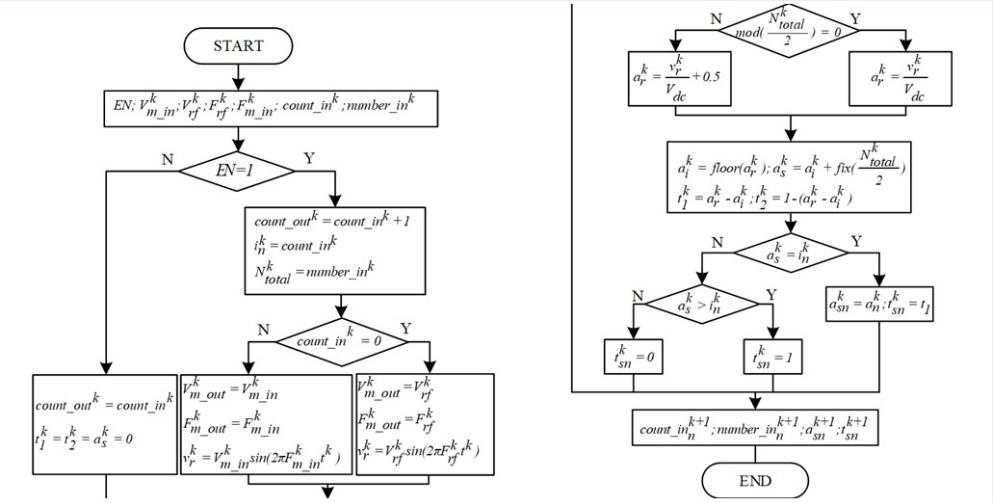

Figure 5: Algorithm flowchart of one cell controller

Table 1: Function of Input and Output in one Cell.

Symbol	Function
count_in	Received the position index of the left cell
number_in	Received the total cells from cell_n+1
Vm_in	Received the amplitude of vr from left cell
Fm_in	Received the frequency of vr from left cell
EN	Enable (active/inactive of cell)
clkin	Received synchronous clock pulse from master cell
count_out	Send the position index to right cell
number_out	Send the total cells to cell_n-1
Vm_out	Send the amplitude of vr to right cell
Fm_out	Send the reference frequency to right cell
clkout	Send the synchronous clock pulse to others cell
Bn, Hn	The cell's PWM control signals.

Table 2: Simulation Parameters.

Parameter	Symbol	Unit	Value
Load	L	mH	4
	R	W	100
Voltage source	$V_{dc}/2$	V	40
Switching frequency	f_{ws}	kHz	10
Sampling time	T_s	s	10^{-6}

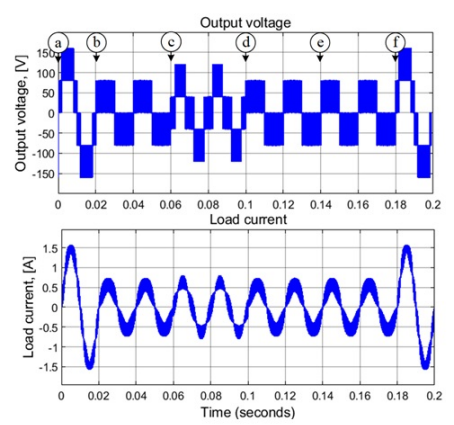

Figure 6: Response of output voltage and load current for a stepwise change of the modulation index and the total number of cells (F_{rf} = 50Hz). (a) M = 0.9375, 4-cell system; (b) M = 0.375, 4-cell system; (c) M = 0.375, 3-cell system; (d) M = 0.375, 2-cell system; (e) M = 0.375, 4-cell system; (f) M = 0.9375, 4-cell system.

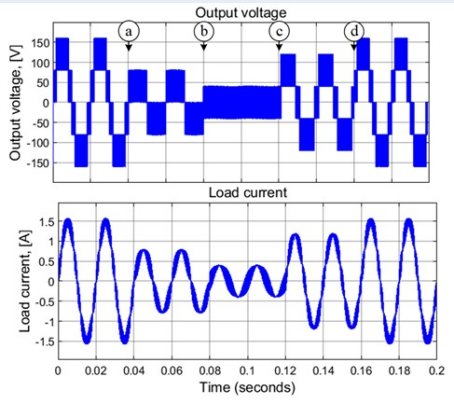

Figure 7: Response of output voltage and load current in case of reconfiguration (F_{rf} = 50Hz, M = 0.9375). (a) removing cell_3,4; (b) removing cell_1; (c) reinserting cell_1,3; (d) reinserting cell_4.

cell_1 is removed, and the output voltage has two levels: 40V and -40V. Cell_1 is replaced by cell_2 to perform the function of a master cell. At 0.12 seconds, cell_1 and cell_3 are reinserted. DPC has 3 cells, and the output voltage has 4 levels. Cell_1 becomes the master cell again. Finally, at 0.16 seconds, cell_4 is reinserted, and the output voltage has 5 levels similar to the starting time. The output voltage can be adjusted according to the output voltage requirements. It will increase or decrease corresponding to 0.5 times of cell voltage, and the system can operate with only 1 cell.

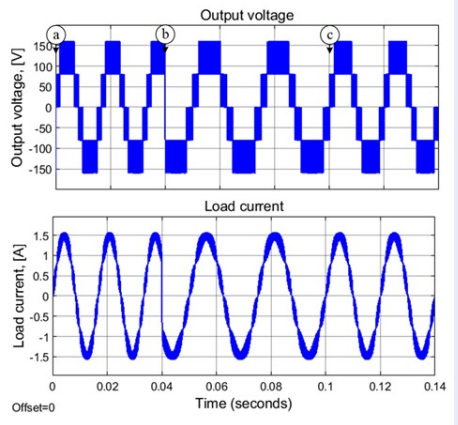

Figure 8: Output voltage and load current waveforms for a stepwise change of the reference voltage frequency M = 0.9375; (a) F_{rf} = 60Hz; (b) F_{rf} = 40Hz; (c) F_{rf} = 50Hz

Figure 8 shows the frequency response to the frequency of the reference voltage. The simulation was performed with all 4 cells in the inverter active and a reference voltage amplitude of 150V. When DPC starts, the frequency of the reference voltage is 60Hz. At 0.04 seconds, the frequency of reference voltage is reduced to 40Hz. Finally, at 0.1 seconds, the frequency of the reference voltage is 50Hz. The DPC output voltage has 5 levels and responds well to changes in the reference frequency.

5. EXPERIMENTAL RESULTS

Experimental prototype as show in Figure 9. Each cell of the DSVPWM consists of DSP controller, driver, and Insulated Gate Bipolar Transistor (IGBT) power cell. Each cell uses one DSP (C2000 Delfino MCUs F28379D) as a controller. The power circuit of each cell includes 2 IGBTs (GW40N120KD). Hybrid integrated IGBT driver MORNSUN QP12W08S-37 is used as the driver circuit. The experiment was conducted with the same parameters as in the simulation in Table 2, with the sampling time adjusted to be 50 ms. The MSPDPC is built with a dynamic connection structure as shown in Figure 1.

In the experimental model, the DSPs are connected to each other by a diagram as shown in Figure 10. For each cell, the input and output signal information on the DSP are presented in Table 3. In the study[19], cell information is exchanged using the GPIO, DAC, and ADC pins on the DSP. However, if the total number of cells in a single-phase inverter increases, a large number of signal pins will be required, which can be dif-

ficult. Additionally, there is a risk of noise and signal amplitude loss during transmission and receiving. In this study, information about cell location and total number of cells is exchanged using the SCI. In each cell, SCIC (GPIO_105) is used to receive the amplitude of the reference voltage transmitted from the left cell, while SCID (GPIO-56) transmits the modulated voltage amplitude to the next cell. Meanwhile, SCID (GPIO-139) and SCIC (GPIO_104) are used to receive and transmit information about the frequency of the modulated voltage. Cell_1 is the master cell, so the received cell values are not considered.

An illustrative experimental result of the ordinal arrangement of cells is shown in Figure 11. The inverter is started with all 4 cells. When cell_1 is removed, the system automatically assigns new sequence numbers for the cells after a 720us interval. When cell_3 of the converter is removed, the DPC has cells_1, 2, 4, and the cells automatically adjust the appropriate PWM signal. The PWM signals of all cells work synchronously, providing an accurate response to the reference voltage frequency.

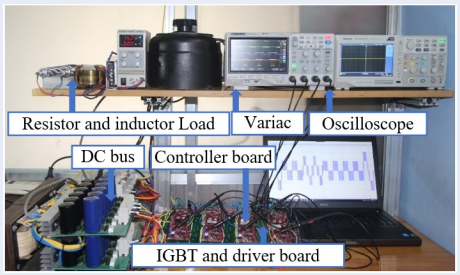

Figure 9: Experimental prototype for the DSVPWM methods

When MSPDPC has four cells, the aggregate voltage of the cells and load current is shown in Figure 12. Figures 13, 14 and 15 show the combined voltage and load current of the remaining cells in the case of dynamic reconfiguration. Specifically, Figure 13 shows that when removing cell_4, the system takes about 0.5ms to reach a new steady state. The number of levels of the output voltage changes from 5 to 4, and the switching voltage is 80V. Similar experimental results are illustrated in Figure 14 when cell_4 is reinserted one after another; the system takes about 0.5ms to stabilize in the new configuration. Figure 15 shows the output voltage and load current in the case of removing cell_1, where the inverter has 2 cells. The output voltage has 2 levels of {40V, -40V}, and the inverter can completely operate with only one cell.

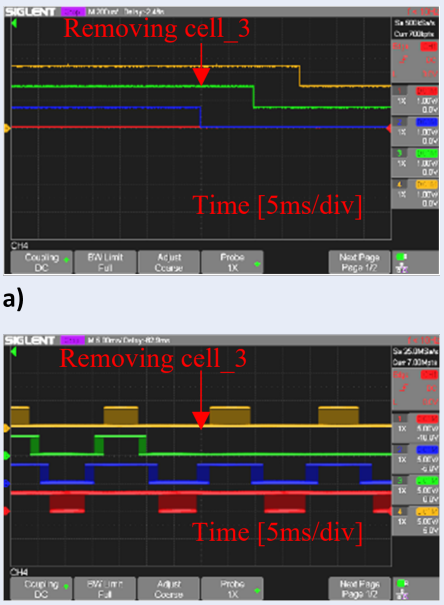

Figure 11: The cell position and PWM control signals of cells in the system. (a) cell position; (b) PWM signals of cells

The aggregate voltage of the cells in the inverter was analyzed using FFT on an oscilloscope (Siglent SDS1104X). The FFT spectrum of the output voltage in the frequency range of 0 to 450Hz as represented in Figure 16a. The first harmonic (at a frequency of 50Hz) has an effective amplitude of 101.6V. Figure 16b presents the results of the voltage spectrum analysis in the frequency range of 0 to 45kHz. The harmonics at 10kHz have an effective value of 23.8V. Additionally, Figure 16 shows that the period of the output voltage is 19.97ms, and the output voltage frequency is 50.08Hz. The results show that the modulation voltage error is 4.4V, equivalent to 4.15%; and the modulation frequency error is 0.08Hz, equivalent to 0.16%.

The modulation technique called DSVPWM for a single-phase multilevel power converter[23] can only handle the issue of an odd-numbered output voltage level. This happens when a cell is either added or removed, leading to an output voltage level that is always odd. voltage with any level, thus enabling more flexible voltage control.

To address this issue, the study proposes a new algorithm for the half-bridge structure that allows for modulation of the output. Additionally, the proposed topology and information exchange between cells

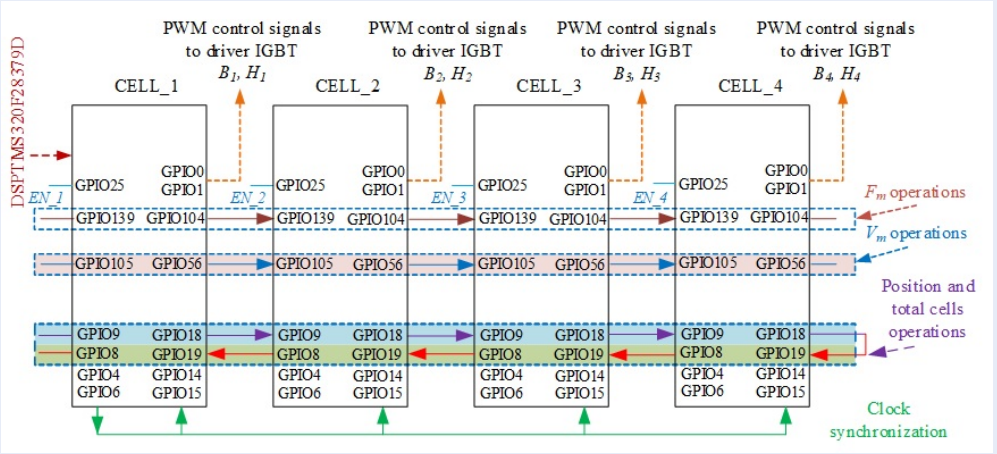

Figure 10: Experimental connection diagram for MSPDPC

Table 3: Function of control pins of DSP

Symbol	Pin on DSP	Parametter
EN	GPIO_25	Enable
V_{m_in}	GPIO_105	Received the amplitude of vr from previous cell
V_{m_out}	GPIO_56	Transmitted the amplitude of vr to next cell
F_{rf_in}	GPIO_139	Received the reference frequency from the previous cell
F_{rf_out}	GPIO_104	Transmitted the reference frequency to the next cell
count_in	GPIO_9	Received index of cell from the previous cell
count_out	GPIO_18	Transmitted index of cell to the next cell
number_in	GPIO_19	Received the total cells
number_out	GPIO_8	Transmitted the total cells
clk_{in}	GPIO_14	Received synchronous clock pulse PWM from master cell
	GPIO_15	Received synchronous clock pulse of vr from master cell
clk_{out}	GPIO_06	Transmitted synchronous clock pulse PWM to others cell
	GPIO_04	Transmitted synchronous clock pulse of the vr to others cell
Bn	GPIO_0	The PWM control signalof cell_n
Hn	GPIO_1	The PWM control signal of cell_n

simplify the calculation process involved in determining the switching vector and corresponding switching time, compared to what is required in Nguyen *et al.* (2022)[23].

6. CONCLUSIONS AND DISCUSSION

This article introduces a decentralized control approach that applies a multilevel SVPWM technique to the half-bridge power converter structure. With this proposed structure, cells can exchange data with their two neighboring cells, including cell position, total number of cells, control voltage frequency, and amplitude. The cells can also automatically determine and select the appropriate switching vector and time. This approach demonstrates that the number of connections required is minimal, improving the operation and control's reliability. The program execution is simple, allowing small processors to operate efficiently. Additionally, this study has improved the algorithm to calculate the cell position and the total

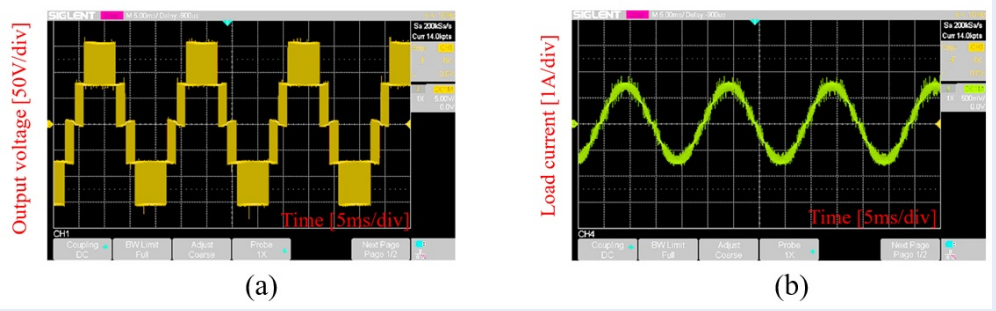

Figure 12: Experimental result for 4-cells system (F_{rf} = 50Hz, M = 0.9375). (a) output voltage waveform; (b) load current waveform.

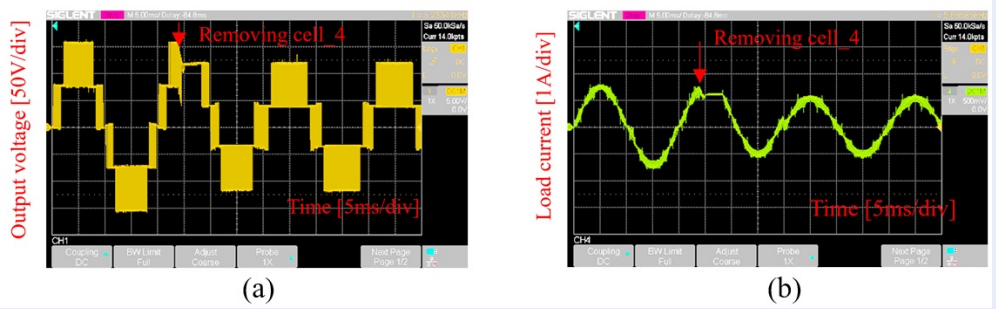

Figure 13: Response of output voltage and load current when removing cell_4 of 4-cell system (F_{rf} = 50Hz, M = 0.9375). (a) output voltage waveform; (b) load current waveform.

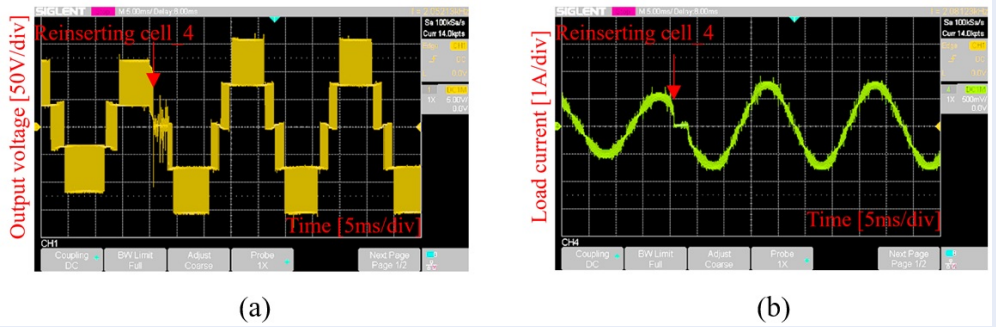

Figure 14: Response of output voltage and load current when reinserting cell_4 of 3-cell system (F_{rf} = 50Hz, M = 0.9375). (a) output voltage waveform; (b) load current waveform

number of cells in the DPC. The structure also allows the MSPDPC to function when only one cell remains. The effectiveness of the proposed algorithm and DSVPWM structure has been confirmed through simulation on Matlab/Simulink software and an experimental model. The MSPDPC has the capability to reconfigure itself dynamically when initiating or dropping one or few cells, a crucial and prominent feature in constructing DPCs.

7. ACKNOWLEDGMENTS

We acknowledge the support of time and facilities from Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for this study.

8. LIST OF ABBREVIATIONS

PWM: Pulse Width Modulation

SVPWM: Space Vector Pulse Width Modulation

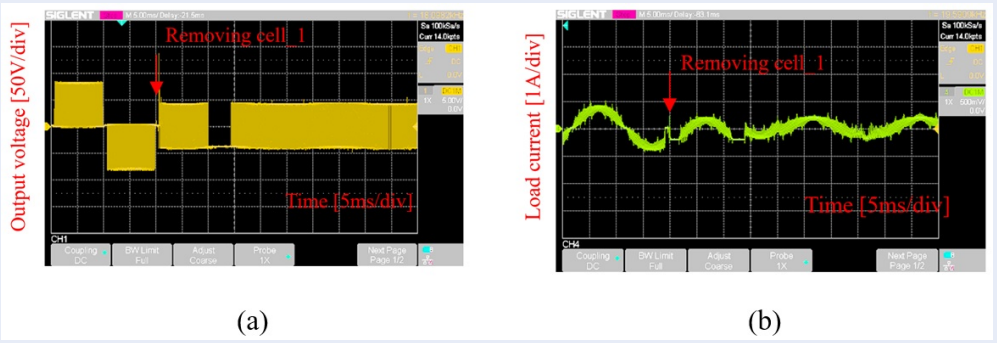

Figure 15: Response of output voltage and load current when removing cell_1 of 2-cell system (F_{rf} = 50Hz, M = 0.9375). (a) output voltage waveform; (b) load current waveform.

Figure 16: Fast Fourier transform (FFT) analysis of the output voltage. (a) Evaluated from 0 to 450 Hz; (b) Evaluated from 0 to 45 kHz.

DPC: Decentralized Power Converter
MSPDPC: Multilevel Single-Phase Decentralized Power Converter
DSVPWM: Decentralized Space Vector Pulse Width Modulation
DSP: Digital Signal Processor
FFT: Fast Fourier Transform
IGBT: Insulated Gate Bipolar Transistor

9. COMPETING INTERESTS

The authors declare that they have no competing interests.

10. AUTHOR CONTRIBUTIONS

Phu Cong Nguyen was responsible for proposing the model, analyzing the structure, and constructing the simulation and experimental models.
Quoc Dung Phan contributed by proposing the ideas and methodology, creating the control algorithm, and participating in the writing, editing, and refinement of the article.
Dinh Tuyen Nguyen was in charge of analyzing the simulation results and also participated in the writing, editing, and refinement of the paper.

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Bài nghiên cứu

Phương pháp điều chế độ rộng xung vector không gian cho bộ biến đổi công suất mô-đun bán cầu một pha, đa bậc điều khiển phân tán

Nguyễn Phú Công[1,2,3], Phan Quốc Dũng[1,2,*], Nguyễn Đình Tuyên[1,2]

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TÓM TẮT

Nghiên cứu này trình bày phương pháp điều chế độ rộng xung vector không gian cho bộ biến đổi công suất một pha, đa bậc điều khiển phân tán. Cấu trúc bộ biến đổi công suất một pha được đề xuất bao gồm các mô-đun bán cầu mắc nối tiếp; cấu trúc gồm các mô-đun ghép nối tiếp cho phép điều chỉnh điện áp ngõ ra theo nhu cầu một cách dễ dàng bằng cách thêm hoặc bớt một vài mô-đun. Mô hình và phương pháp điều chế vector không gian phân tán đề xuất sử dụng cấu trúc các mô-đun sẽ trao đổi thông tin với 2 mô-đun lân cận nhằm thực hiện điều chế vector đóng cắt và thời gian chuyển mạch tương ứng. Nghiên cứu tập trung đánh giá khả năng đáp ứng của điện áp ngõ ra theo điện áp tham chiếu, đánh giá khả năng điều chỉnh lại vector đóng cắt và thời gian chuyển mạch tương ứng của mỗi mô-đun khi cấu trúc của bộ biến đổi công suất thay đổi. Khả năng cấu hình lại động của các bộ biến đổi công suất dạng phân tán là một tính năng vô cùng quan trọng; điều này cho này cho phép đảm bảo tính cung cấp điện liên tục trong trường hợp có một hoặc vài mô-đun bị hỏng; hệ thống tự động xác lập trạng thái mới với số lượng mô-đun còn đang hoạt động. Cấu trúc và phương pháp đề xuất có thời gian cấu hình rất nhanh. Cấu trúc bộ nghịch lưu một pha có điện áp ngõ ra được điều chỉnh tương ứng 0.5 lần điện áp mỗi mô-đun, điều này cho phép biên độ điện áp điều chế được điều chỉnh phù hợp nhất theo yêu cầu phụ tải. Nghiên cứu được xác minh tính hiệu quả dựa trên kết quả mô phỏng bằng phần mềm Matlab/Simulink và mô hình thực nghiệm. Tải RL với thông số định mức 220V / 500W được dùng để kiểm chứng kết quả thực nghiệm cho bộ biến đổi công suất điều khiển phân tán năm bậc, một pha.

Từ khoá: Bộ biến đổi công suất đa pha, đa bậc, điều khiển phân tán, điều chế độ rộng xung vec-tơ không gian, tái cấu hình động, bộ biến đổi công suất đa mô-đun ghép nối tiếp và song song, bộ biến đổi công suất các mô-đun bán cầu mắc nối tiếp

[1]*Khoa Điện - Điện tử, Trường Đại học Bách Khoa Thành phố Hồ Chí Minh, Việt Nam*

[2]*Đại học Quốc gia Thành phố Hồ Chí Minh, Việt Nam*

[3]*Khoa CN Điện - Điện tử, Trường Đại học Công nghiệp Thực phẩm Thành phố Hồ Chí Minh, Việt Nam*

Liên hệ

Phan Quốc Dũng, Khoa Điện - Điện tử, Trường Đại học Bách Khoa Thành phố Hồ Chí Minh, Việt Nam

Đại học Quốc gia Thành phố Hồ Chí Minh, Việt Nam

Email: pqdung@hcmut.edu.vn

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